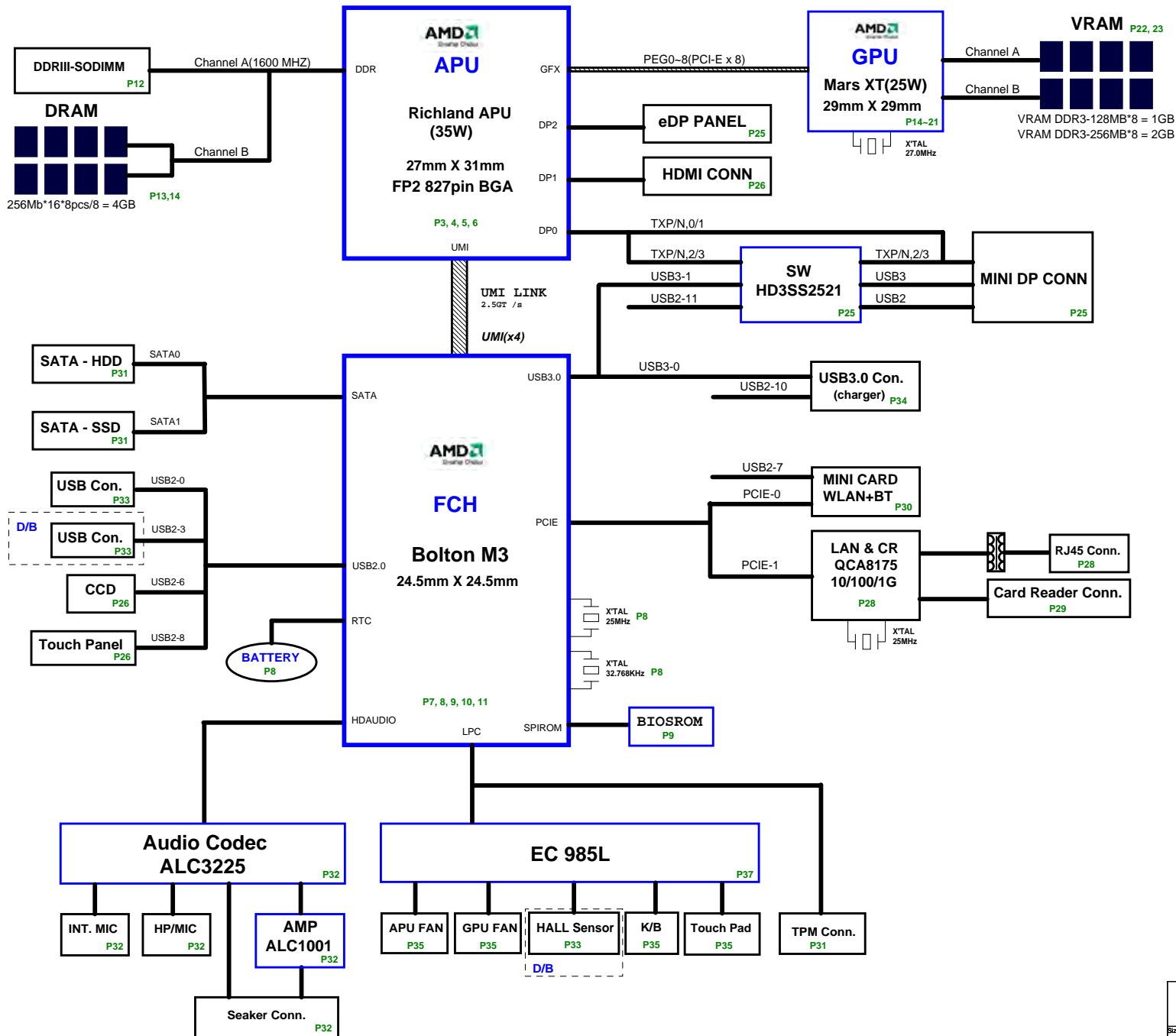


ZRI/ZQI Block Diagram



PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : SVCC
- LAYER 6 : IN3
- LAYER 6 : GND
- LAYER 8 : BOT

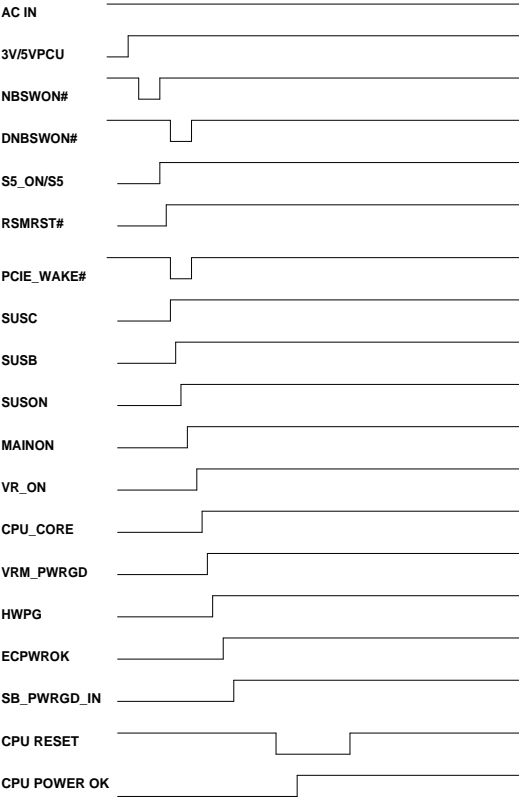
BOM Option

ITEM	DESCRIPTION	MARK
1	LVDS Panel Sku	LVDS@
2	eDP Panel Sku	eDP@
3	VGA Sku	EV@
4	VGA Thames Sku	EV_T@
5	VGA Mars Sku	EV_M@
6	VGA Sku for Thames and Mars stuff different value parts	EV_SP@
7	GPU 128bit Sku	EV_128@
8	GPU 128bit Sku of Special part value change	EV_128SP@
9	USB Charge Functions Sku	CH@
10	No USB Charge Functions Sku	NCH@
11	USB3.0 Re-Driver Sku	RD@
12	No USB3.0 Re-Driver Sku	NRD@
13	Always connect functions Sku	AC@
14	No Always connect functions Sku	NAC@
15	Special part value change or modify for different BOM sku	SP@
16	Key Board Back light Sku	KBL@
17	SSD Sku	SSD@
18	Touch panel Sku	TP@

Page 9 GPIO strap pin

ITEM	DESCRIPTION	MARK
1	Synaptics touch pad	SYNP@
2	ELAN touch pad	ELAN@
3	For UMA Sku	UMA@
4	ELPIDA on board DRAM	ELP@
5	HYNIX on board DRAM	HYN@

Power Sequence



Hudson M3 SMBUS

FCH SMBUS	Pin NO.	SMBUS Function Define
PCLK_SMB PDAT_SMB (+3V)	AD26 AD25	DDR / WLAN
SCLK1 SDATA1 (+3V_S5)	T7 R7	Touch Pad
SMB_EC_CLK (SCLK2) SMB_EC_DAT (SDATA2) (+3V_S5)	H19 G19	EC
SCLK3 SDATA3 (+3VPCU)	G22 G21	Not used
SCL4 SDATA4 (+3V_S5)	J19 K19	Not used

EC SMBUS

KBC SMBUS	Pin NO.	SMBUS Function Define
MBCLK MBDATA (+3VPCU)	70 69	Battery, FCH
APU_SIC_EC APU_SID_EC (+3V_S5)	67 68	APU
GPUP_CLK GPUP_DATA (+3V_GFX)	119 120	GPU
TPCLK TPDATA (+3V)	72 71	Touch Pad

EC	FCH	Device I2C_Device(S)			
I2Ce_1(M)	I2Cf_2(M)	Charger	Battery		ALL/S5
I2Ce_2(M)		APU			ALL
I2Ce_3(M)					
	I2Cf_3(M)	APU			S5
	I2Cf_1(M)				S5
	I2Cf_0(M)	DDR	WLAN/3G	Image Sensor	S0

EC will Conflict with FCH.
Do not mount

PEG X 8

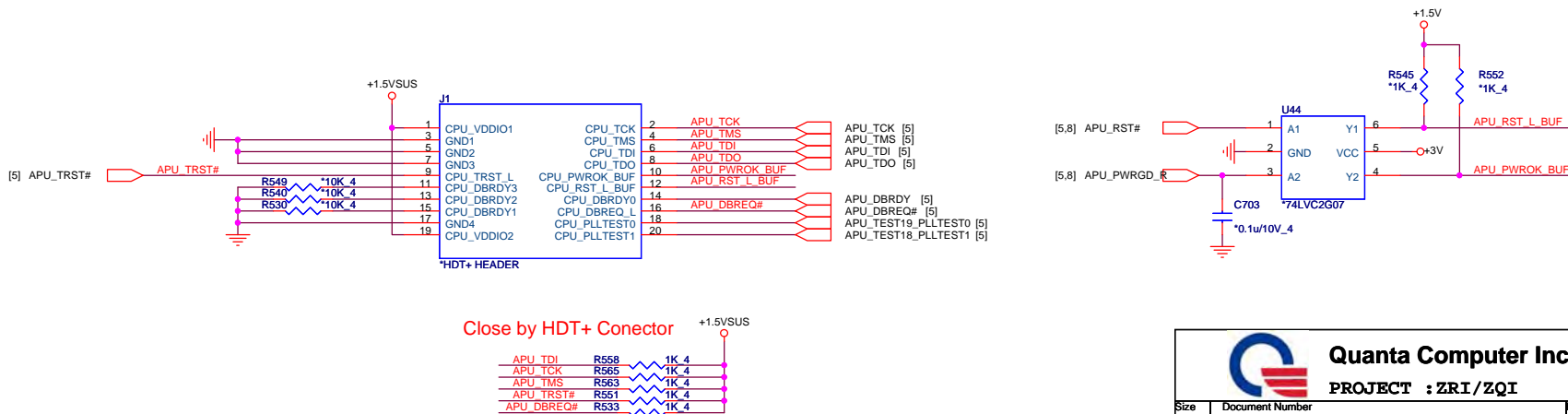
PEG X 8

FP2 only support PEG X 8

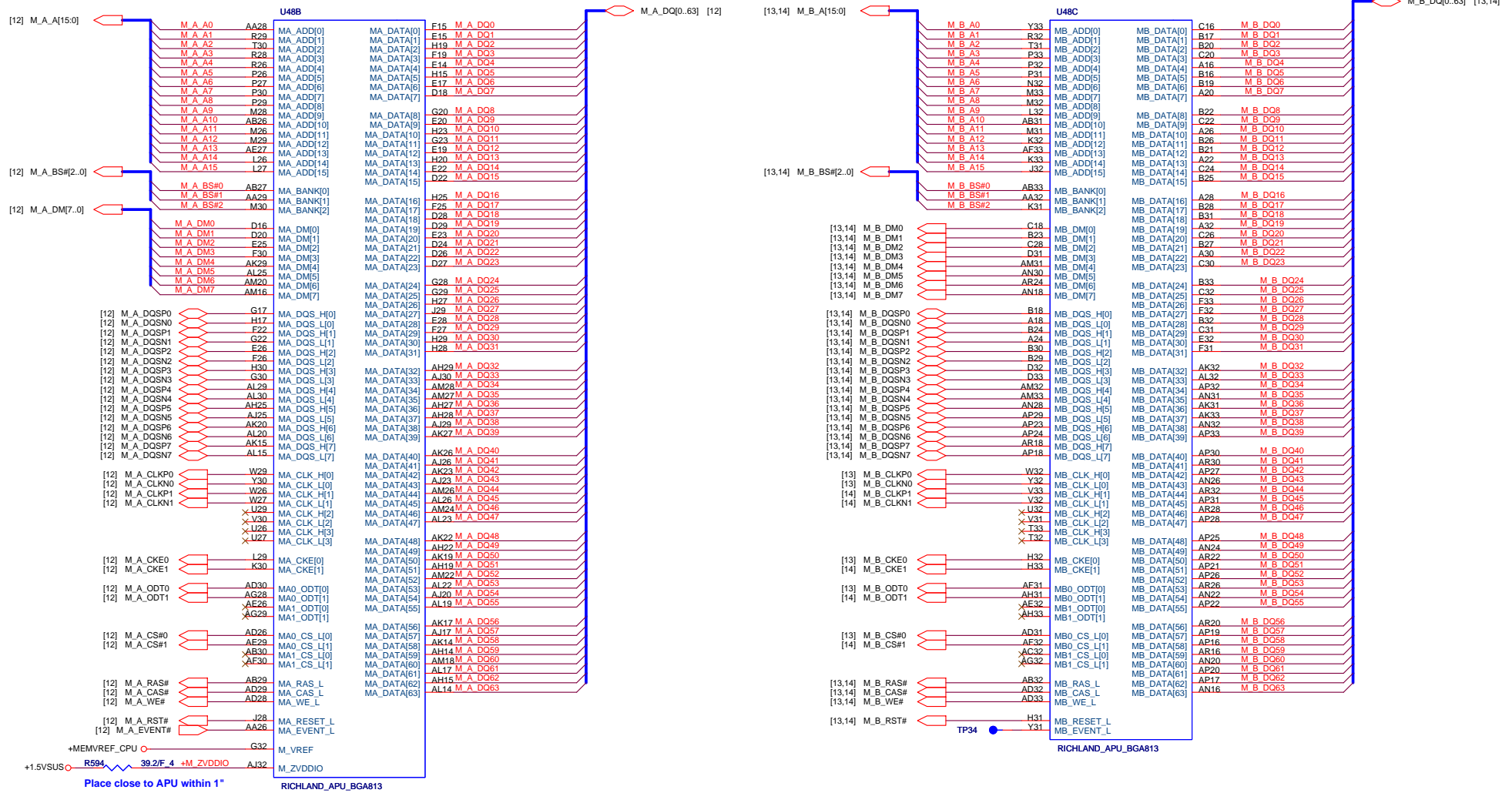
FP2 only support PEG X 8

A10	AJ05757RT01
A8	AJ05557UT01
A6	AJ053578T01

HDT+ Connector for Debug only



Soldermask openings for all bottom side vias/TPs under FS1

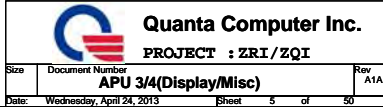


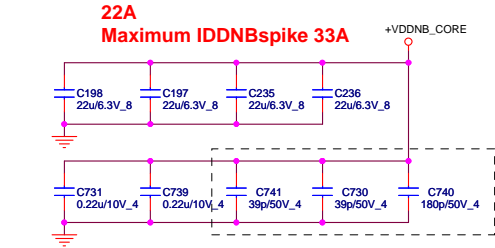
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A6	AJ053578T01

Quanta Computer Inc.
PROJECT : ZRI / ZQI

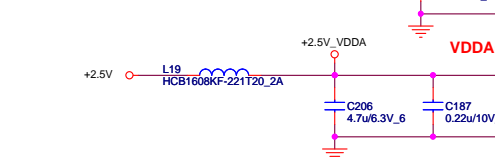
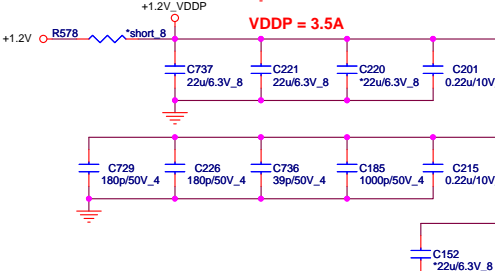
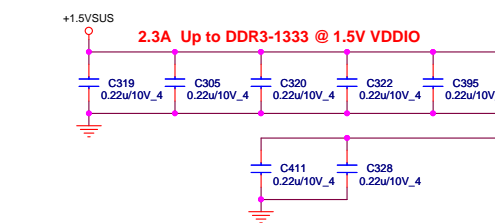
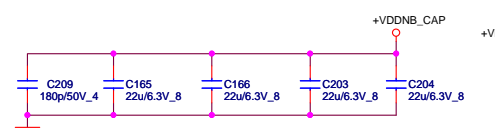
Size	Document Number	Rev
	APU 2/4(DDR3 MEM I/F)	A1A
Date:	Wednesday, April 24, 2013	Sheet 4 of 50

A6	AJ053578T01
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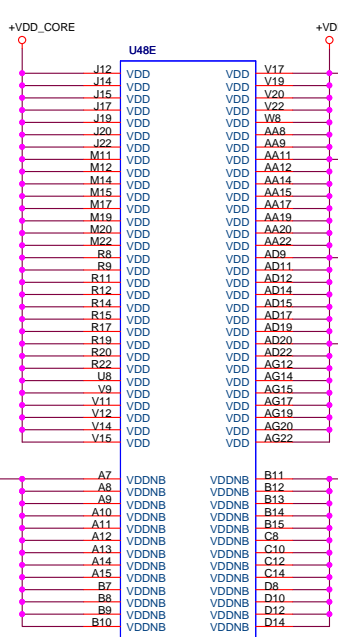




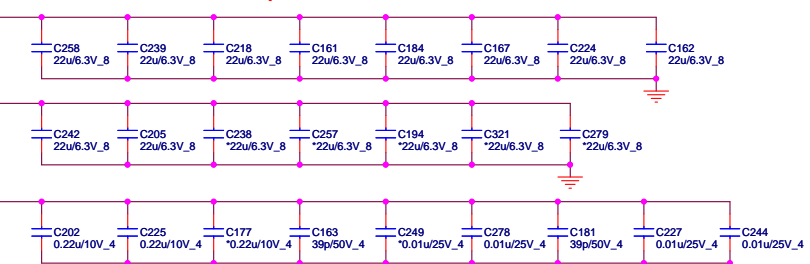
For EMI



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A6	AJ053578T01

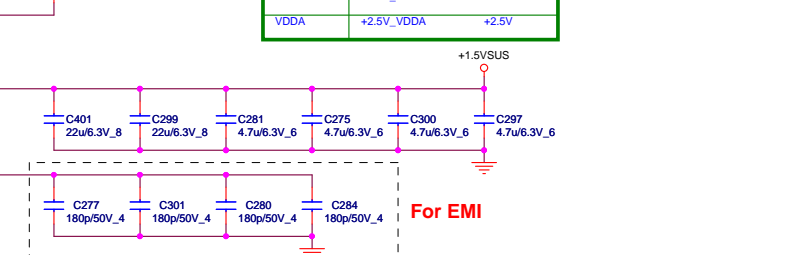


22A
Maximum IDDSpike 35A

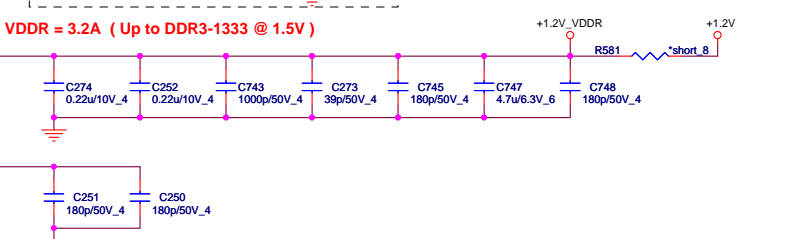


For EMI

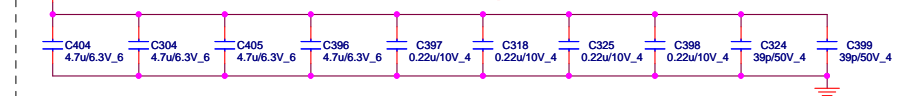
PIN NAME	NET NAME	VOLTAGE
VDD	+VDD_CORE	1.0V ~ 1.3V
VDDNB	+VDDNB_CORE	1.05V ~ 1.325V
VDDIO	+1.5VSUS	1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V



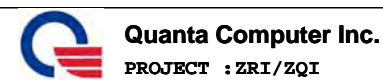
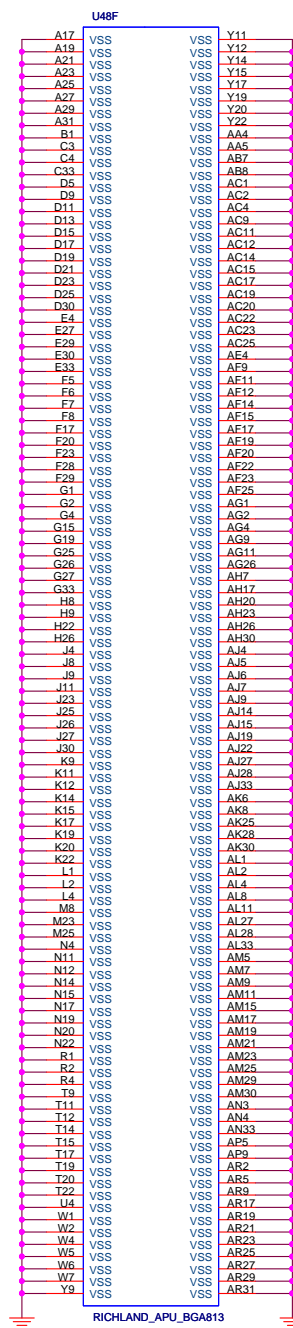
For EMI



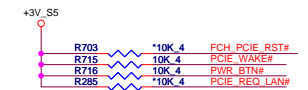
DECOUPLING between PROCESSOR and DIMMs
Across VDDIO and VSS split



If the VSS plane is cut to create a VDDIO plane, ceramic capacitors are connected across the VDDIO and VSS plane split as follows

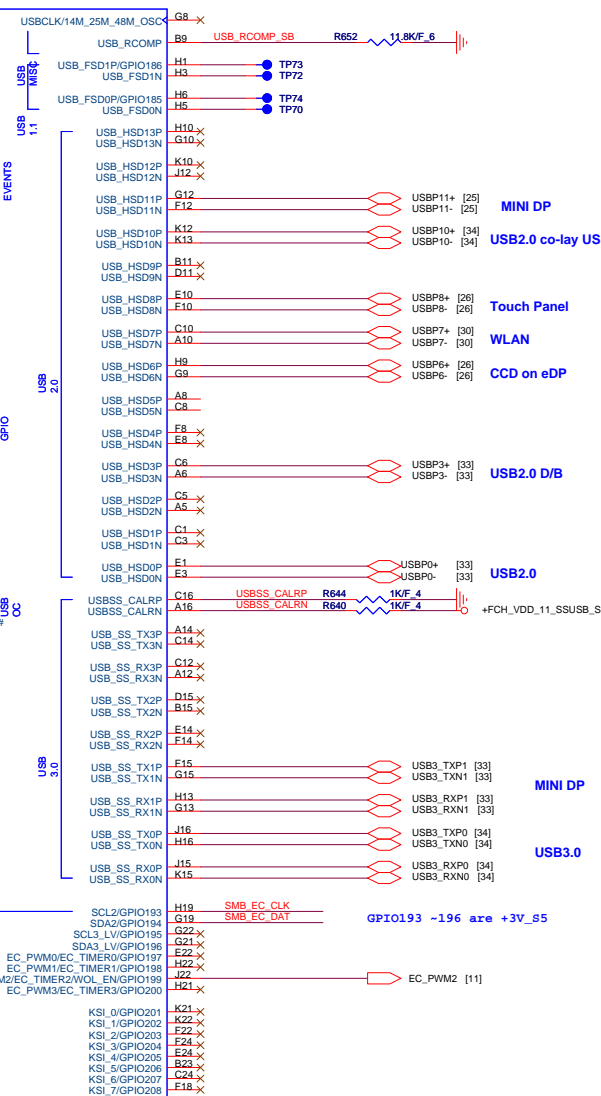
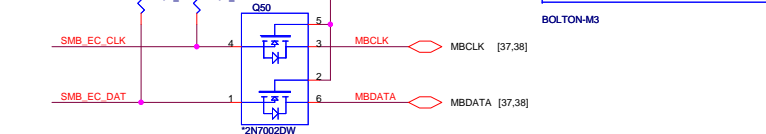
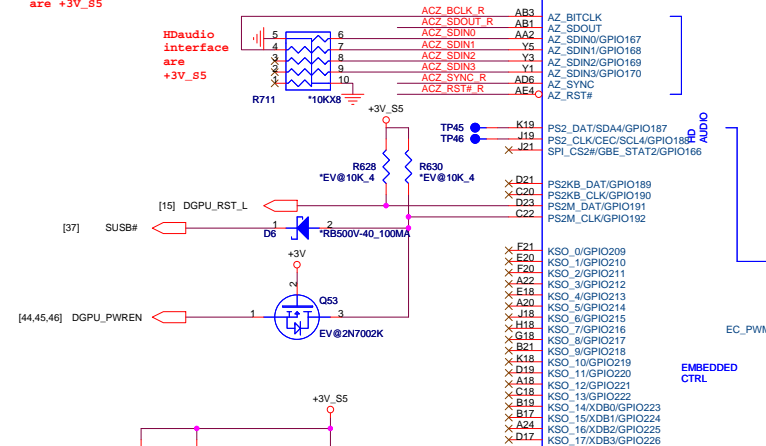
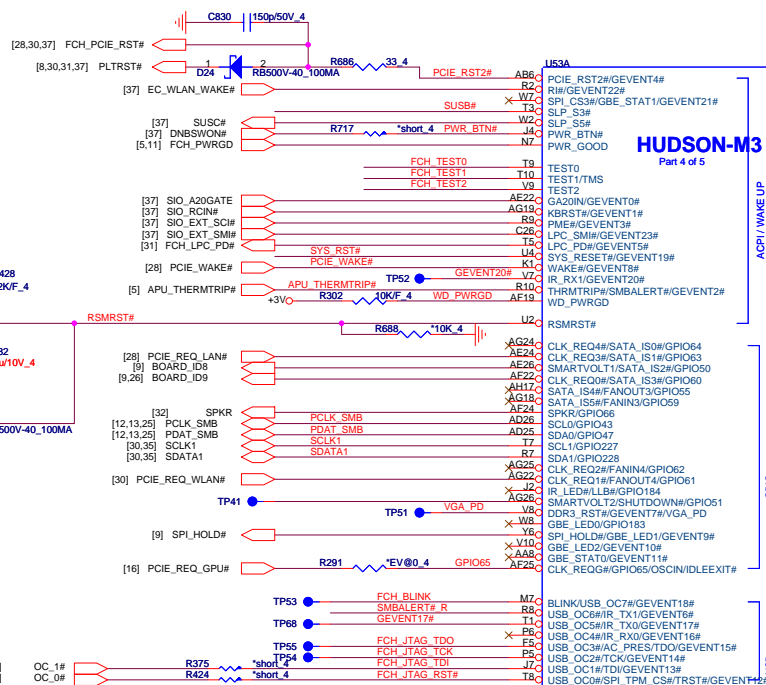
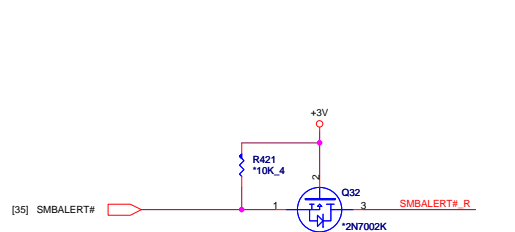
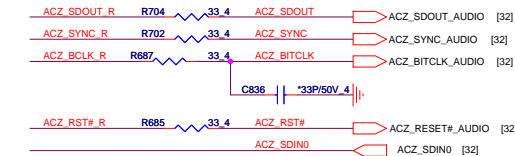


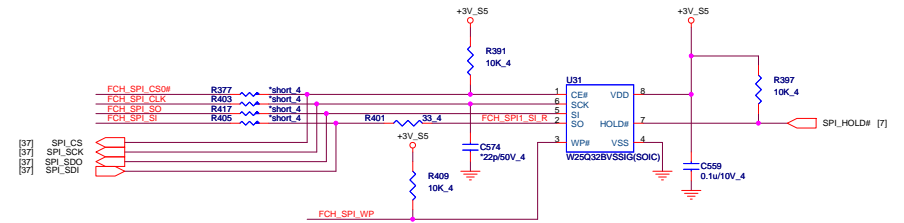
Size	Document Number	Rev
	APU 4/4(Power/GND)	A1A
Date:	Wednesday, April 24, 2013	Sheet 6 of 50

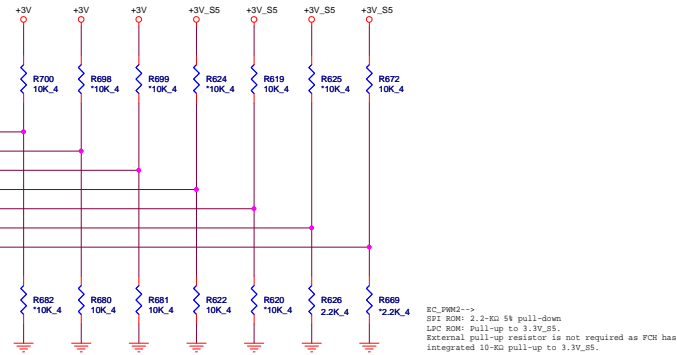


Note: LLB#, WAKE# and PWR_BTN need pull up to +3VPCU only if S5+ mode is supported

To Azalia

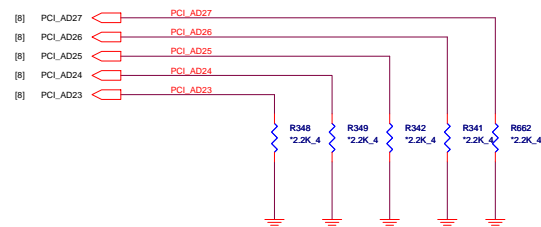




[illegible]

Remove PCI_CLK2 function									
	-----	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	-----	ALLOW PCIe Gen2 DEFAULT	-----	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE ENABLED DEFAULT
PULL LOW	-----	FORCE PCIe Gen1	-----	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

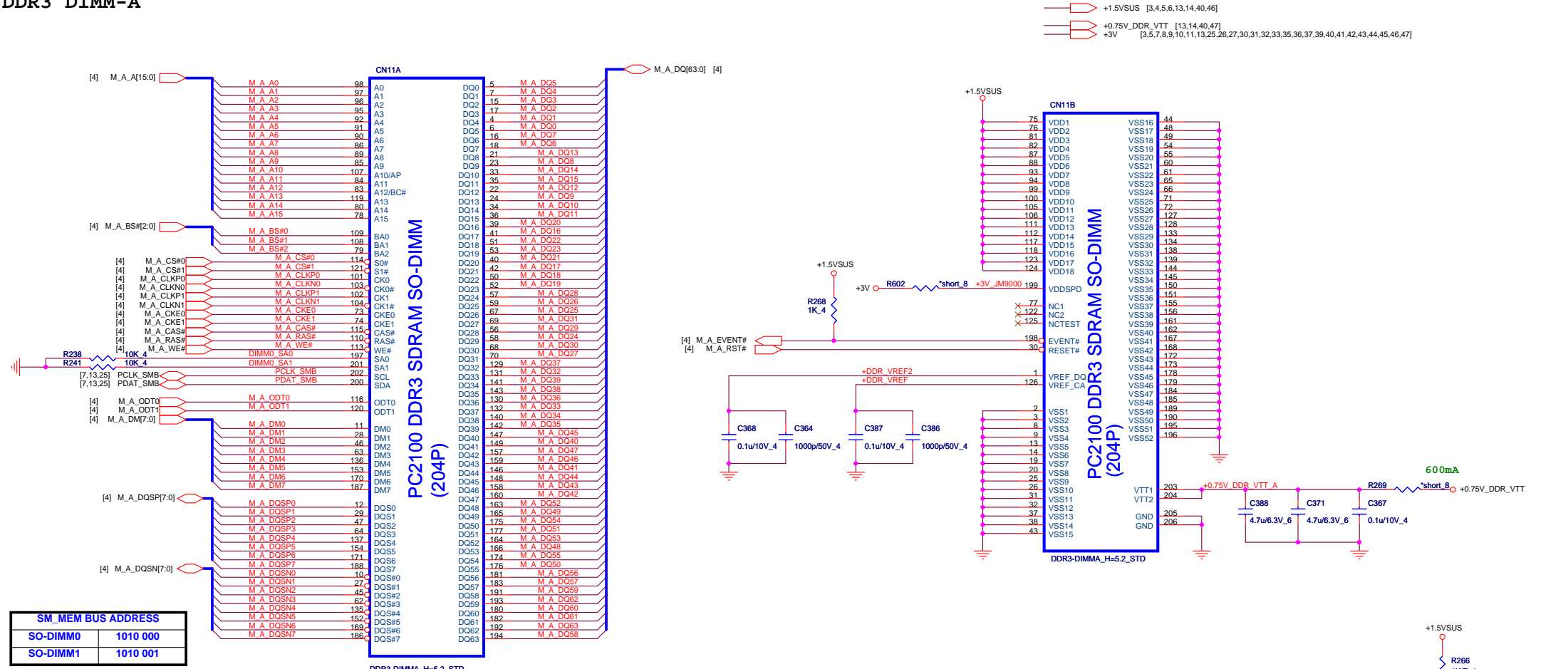
FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]




	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	USE DEFAULT PCIE STRAPS	DISABLE PCI MEM BOOT
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

The schematic diagram shows the FCH_PWRGD signal circuit. It features a +3V supply connected to a 10K resistor (R399) and a 2.2uF capacitor (C564). The output of the capacitor is connected to the input of a Schmitt trigger (U32, SN74VHC1G17DCR). The Schmitt trigger is also connected to a 10.1uF capacitor (C576) and a 0.4 ohm resistor (R422). The output of the Schmitt trigger is connected to the FCH_PWRGD signal and the output of the 0.4 ohm resistor (R422). The input to the Schmitt trigger is also connected to the FCH_PWRGD signal and the output of a 0.4 ohm resistor (R411).

DDR3 DIMM-A



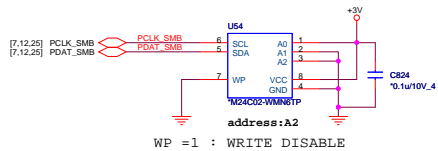
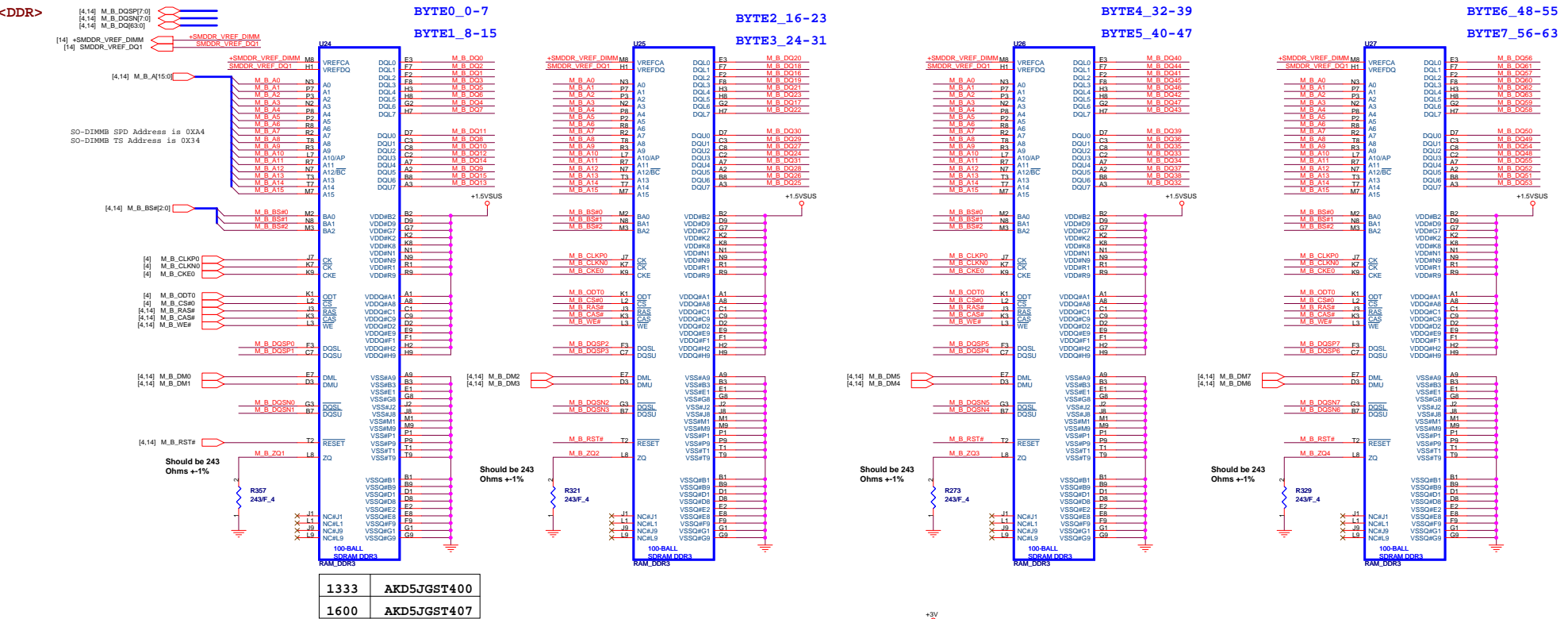


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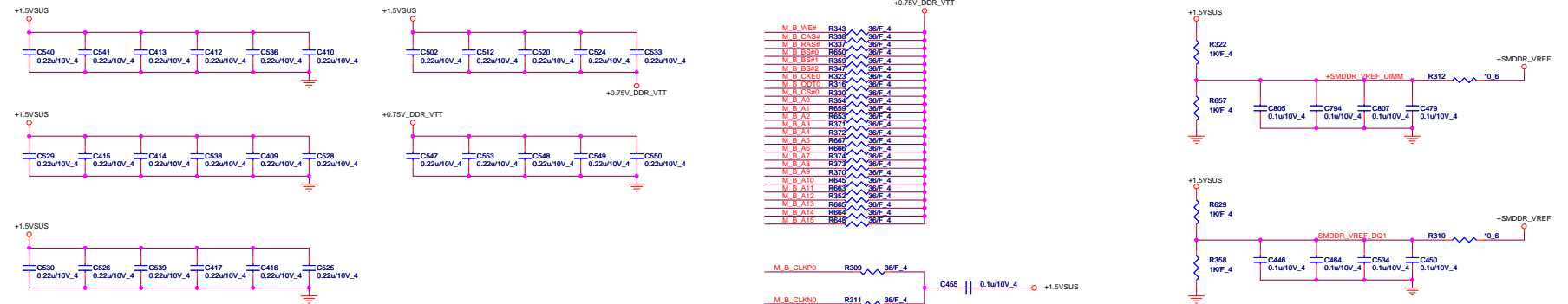
PROJECT : ZRI/ZQI

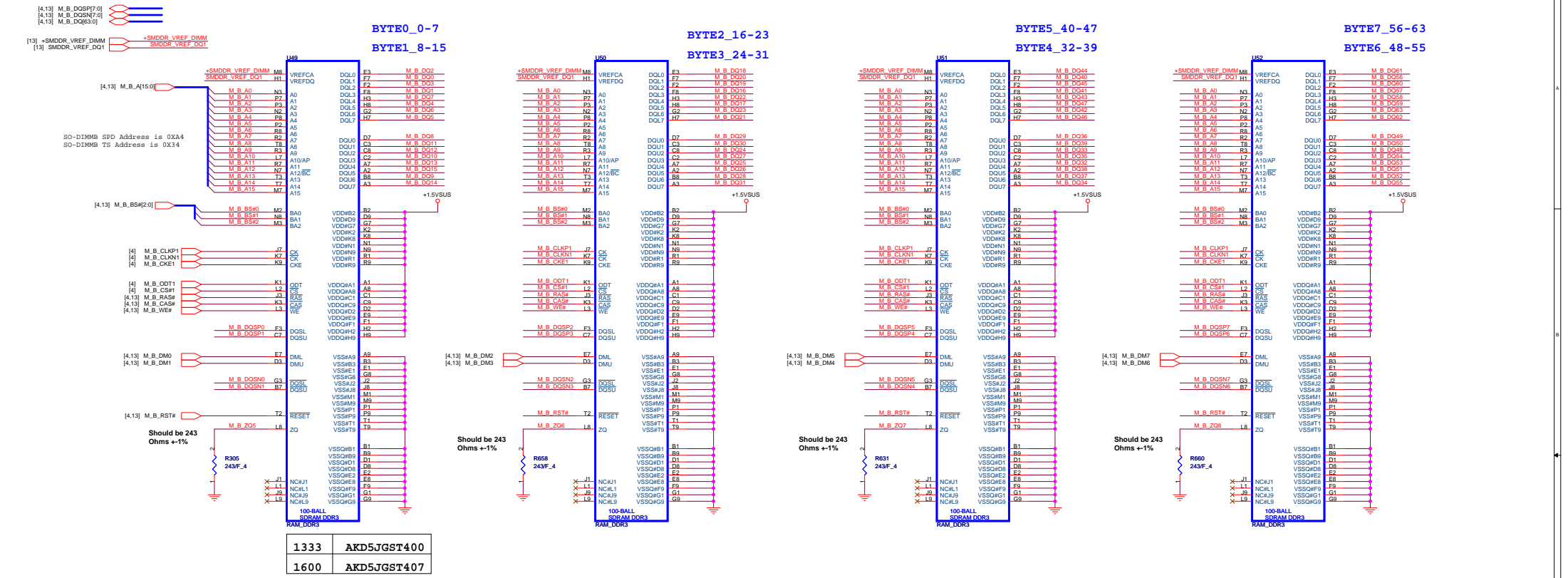
Size	Document Number	Rev
	DDR3 SO-DIMM A	A1A
Date:	Wednesday, April 24, 2013	Sheet 12 of 50

<DDR>

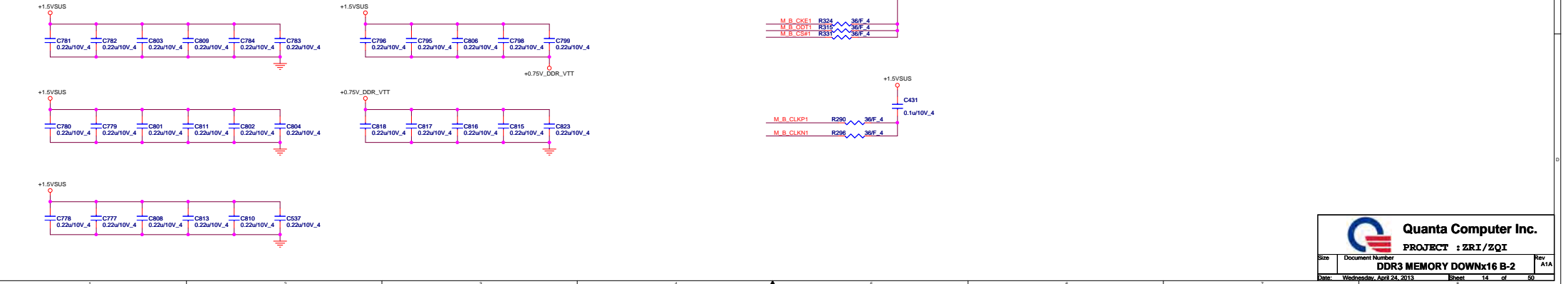


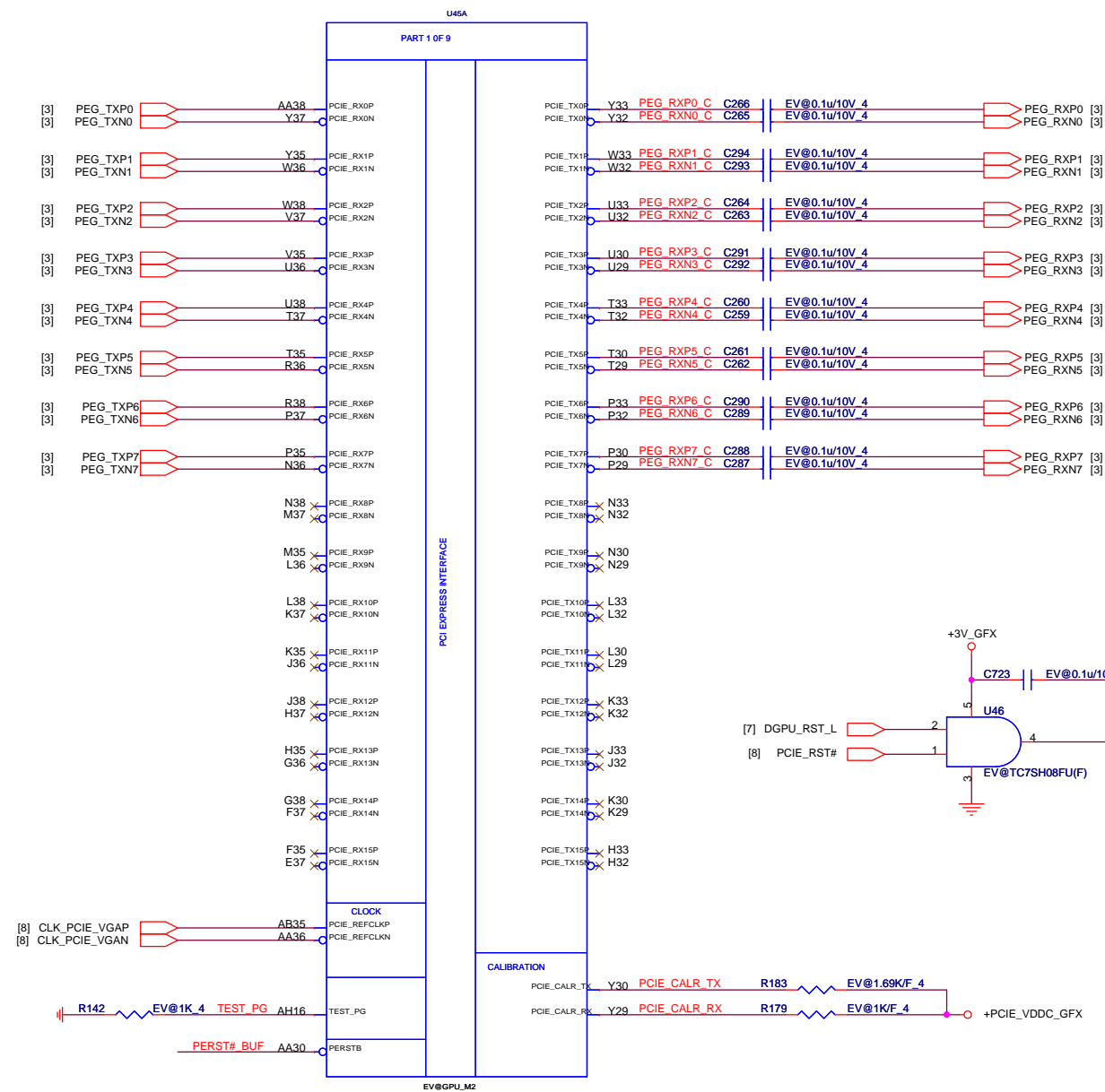
Place these Caps near Memory Down





Place these Caps near Memory Down





Thames(Pro,XT) and Mars Power-on sequence PX5.0(no BACO)

DGPU_PWREN

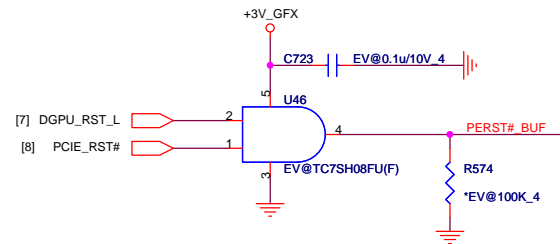
VDDC/VDDCI/1.8V_IO
MVDDQ/+PCIE_VDDC
VDDR3

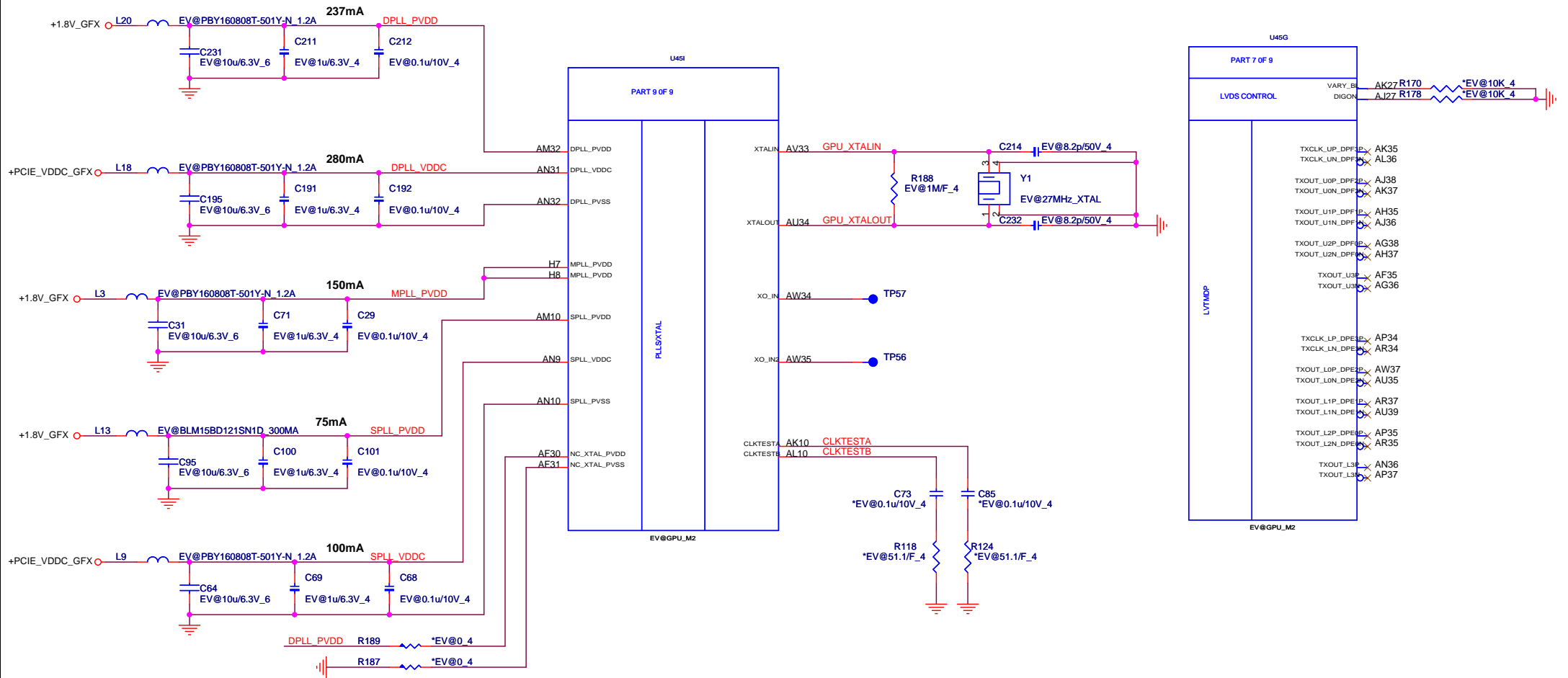
PE_PWRGD

PWRGOOD

PCIE_RST#

PCIE Clock





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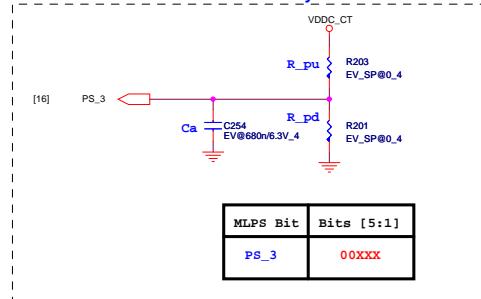
PROJECT : ZRI/ZQI

Size	Document Number	Rev
	Thames M2/ XTAL_LVDS	A1A
Date:	Wednesday, April 24, 2013	Sheet 17 of 50

Vendor	Vendor P/N	STN B/S P/N	Size	MLPS
Hynix	H5TQ2G63DFR-11C (128M*16)	AKD5MGWTW17 * 8	2GB	000
	H5TC2G63FFR-11C (128M*16)	AKD5MZDTW05 * 8	2GB	001
Micron	MT41K256M16HA-107G (256M*16)	AKD5PGSTL05 * 8	4GB	011

Mars USE

SP : Mars DDR3 Memory TYPE Set



MLPS

R_pu	R_pd	Bits [3:1]
NC	4.75K	D 000
8.45K	2K	F 001
4.53K	2K	B 010
6.98K	4.99K	011
4.53K	4.99K	100
3.24K	5.62K	101
3.4K	1M	110
4.75K	NC	111

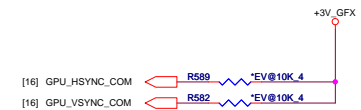
Ra	P/N
2K	CS22002FB19
3.24K	CS23242FB09
3.4K	CS23402FB08
4.53K	CS24532FB08
4.75K	CS24752FB12
4.99K	CS24992FB26
5.62K	CS25622FB18
6.98K	CS26982FB01
8.45K	CS28452FB12
1M	CS51002FB11

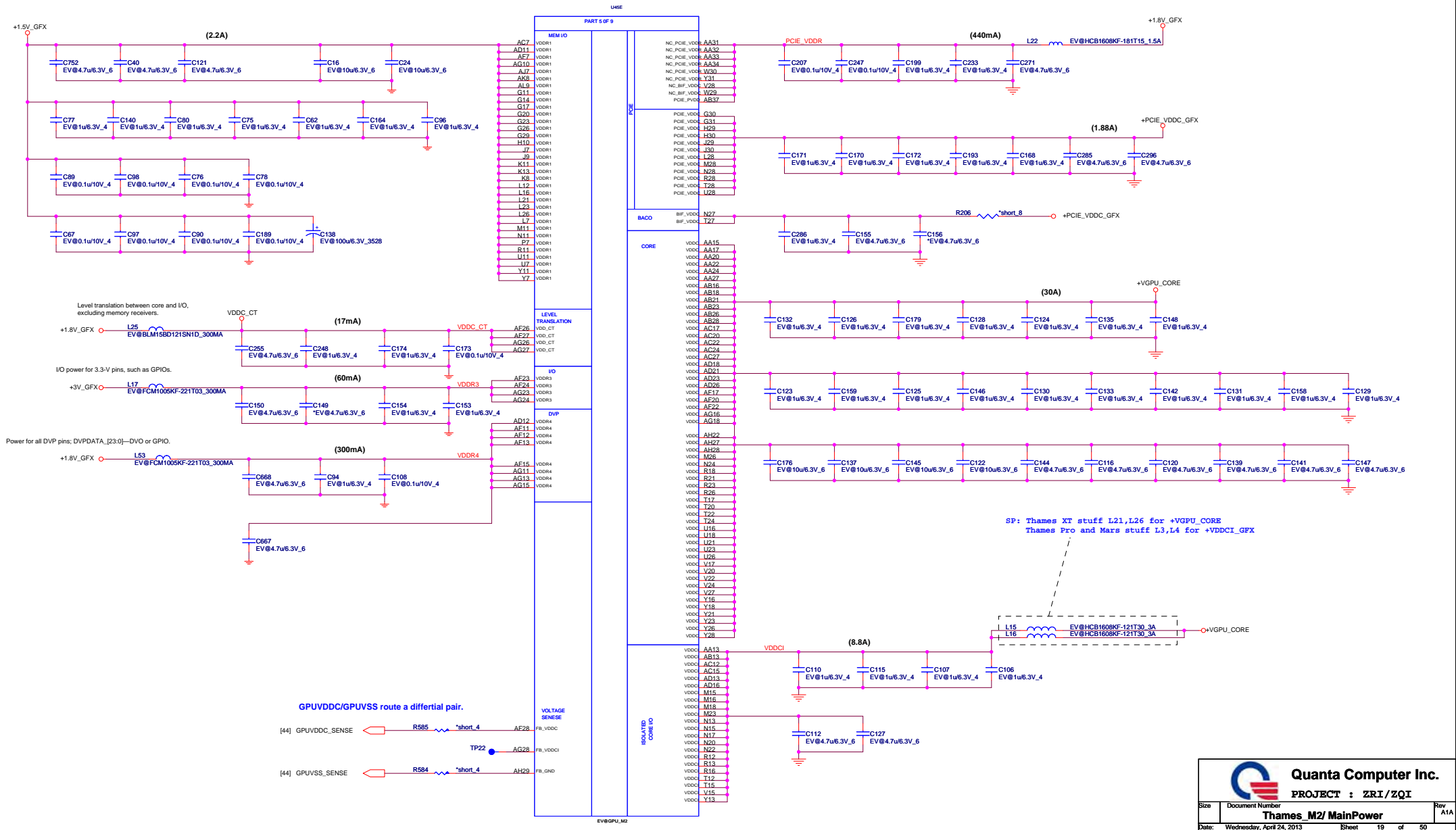
Ca	Bits [5:4]	P/N
680nF	00	CH4681K9B00
82nF	01	CH3823K1B00
10nF	10	CH31003KB11
NC	11	

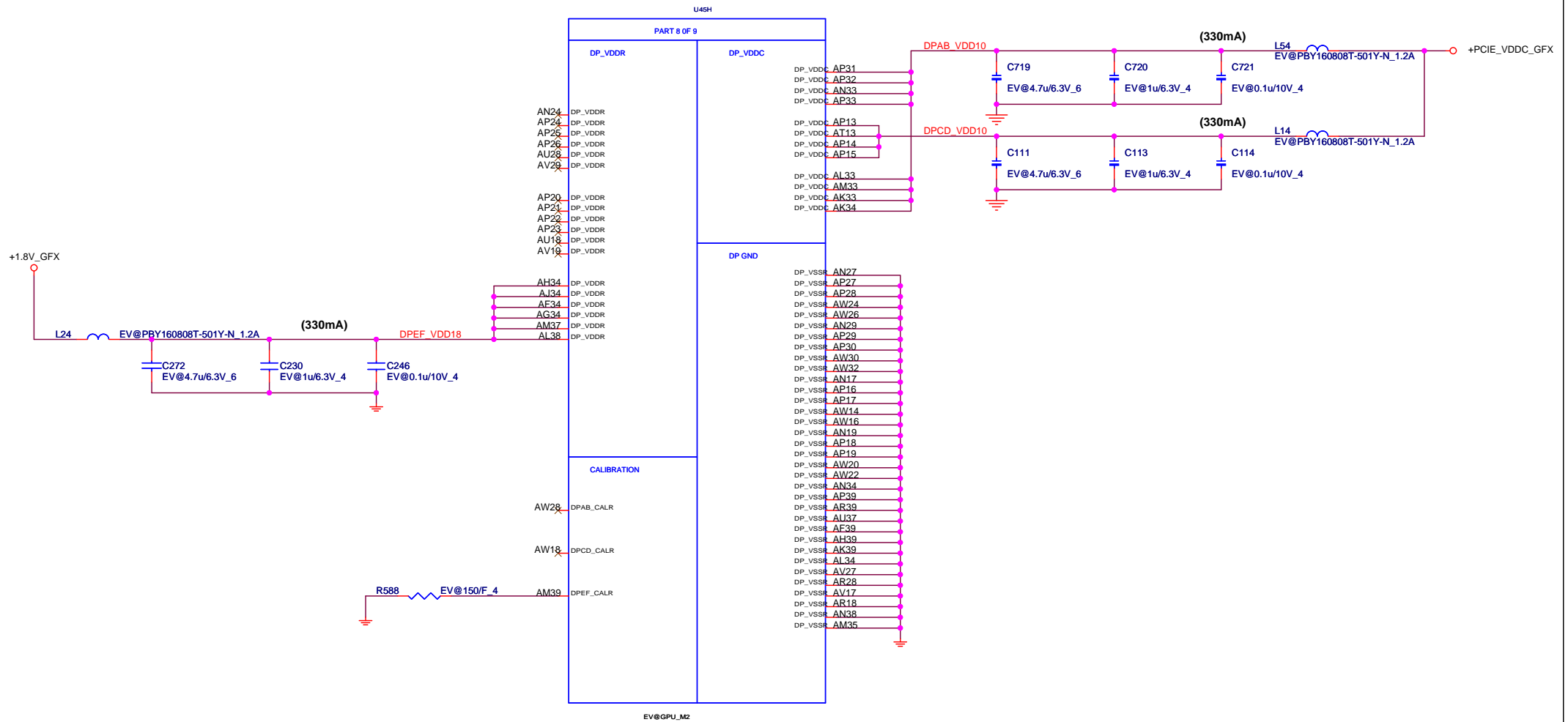
CONFIGURATION STRAPS – SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				Default Setting
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWR5_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIE Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA_DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA	GENLK_CLK GPIO8 GPIO21 GENERICC	NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOs ARE USED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

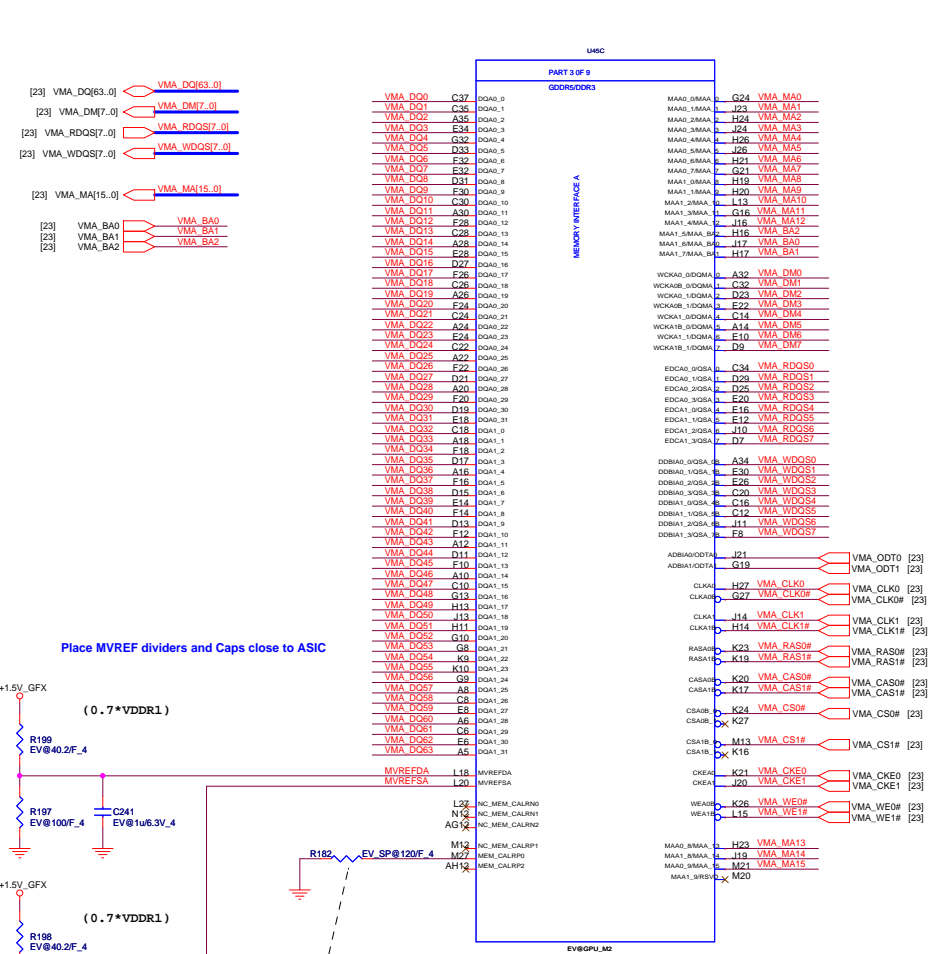
System Memory Aperture size

GPIO9 BIOSROM		GPIO11 ROMIDCFG0	GPIO12 ROMIDCFG1	GPIO13 ROMIDCFG2
0	128M	0	0	0
0	256M	1	0	0
0	64M	0	1	0
0	32M	1	1	0





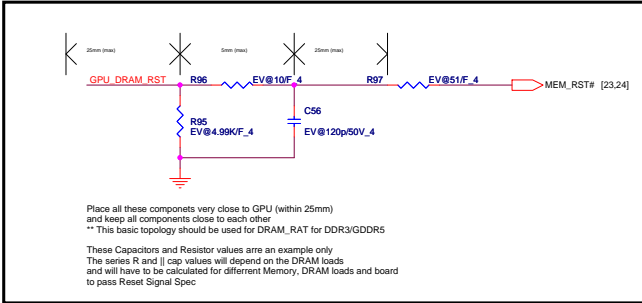
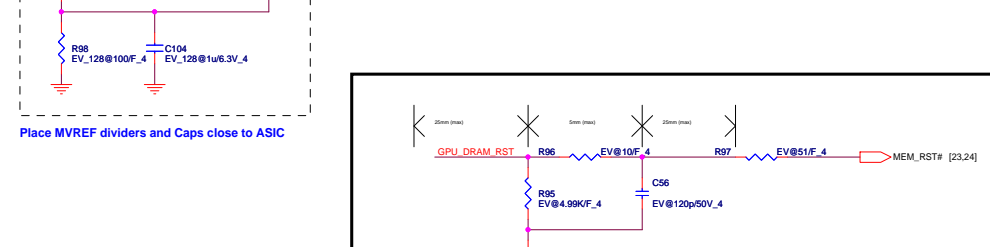
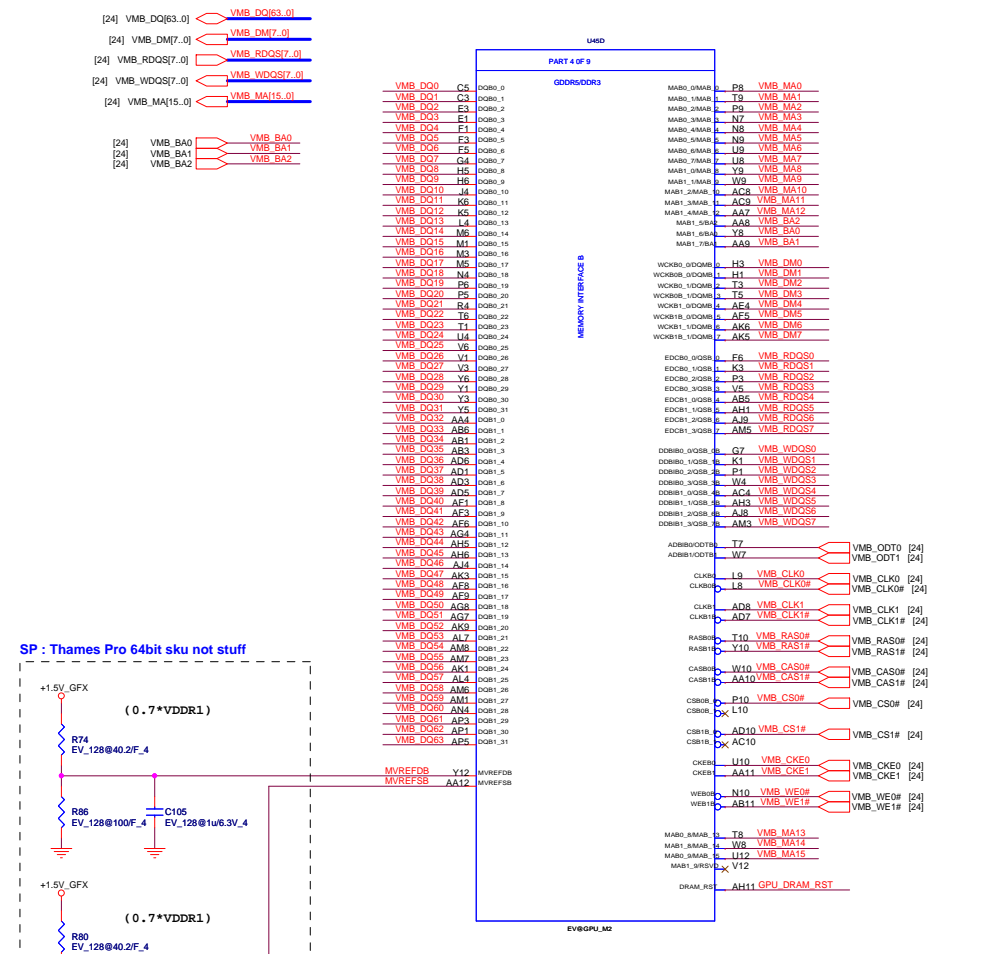




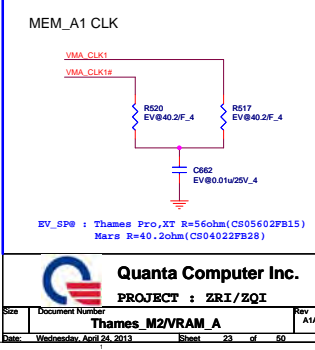
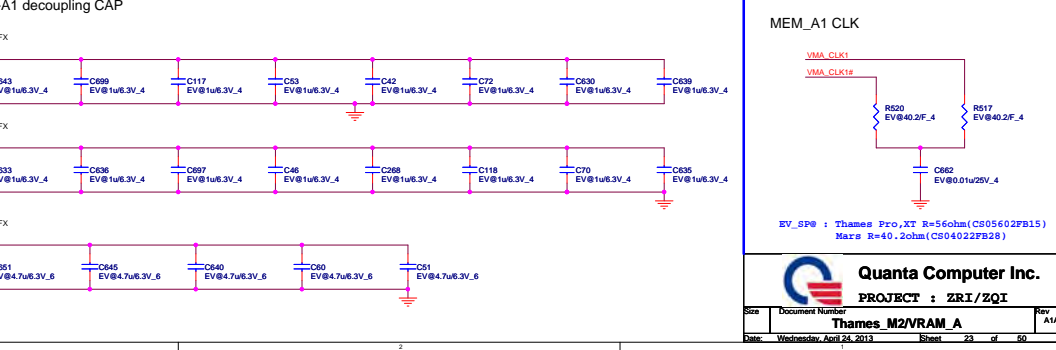
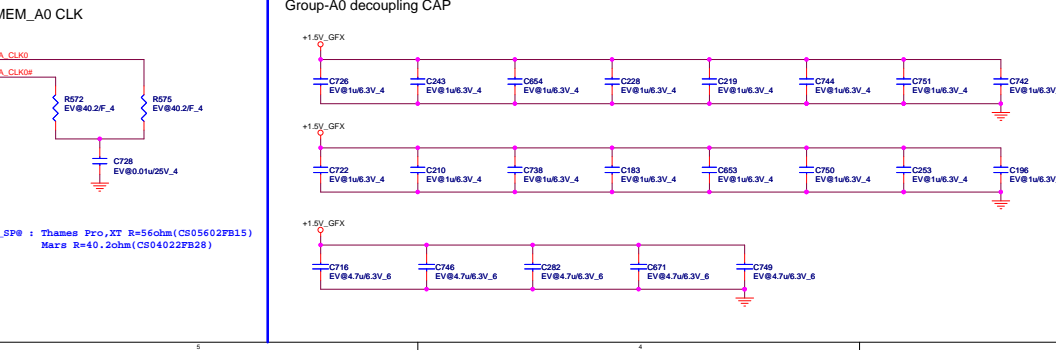
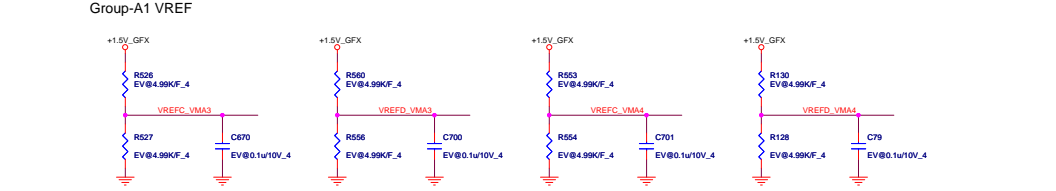
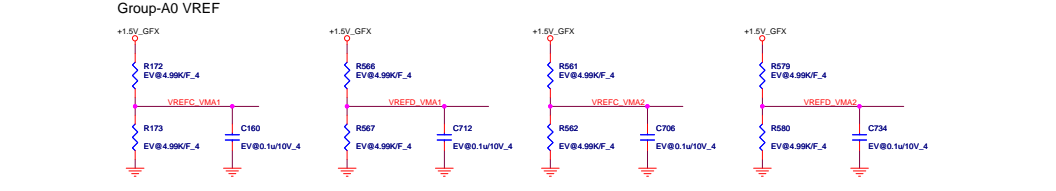
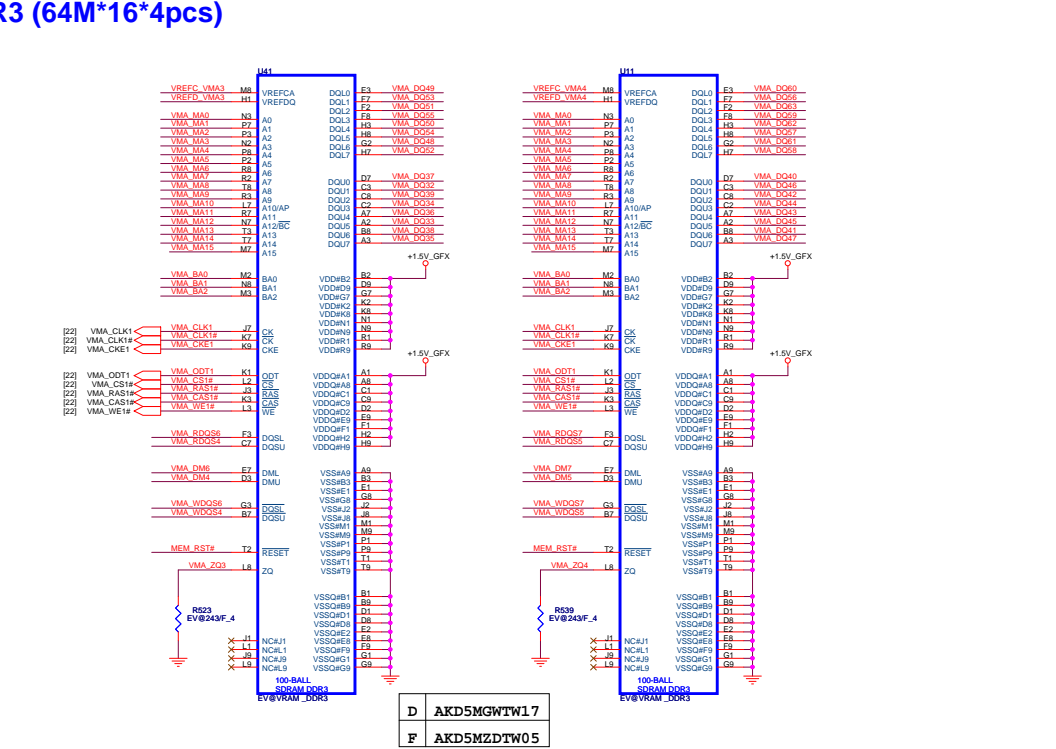
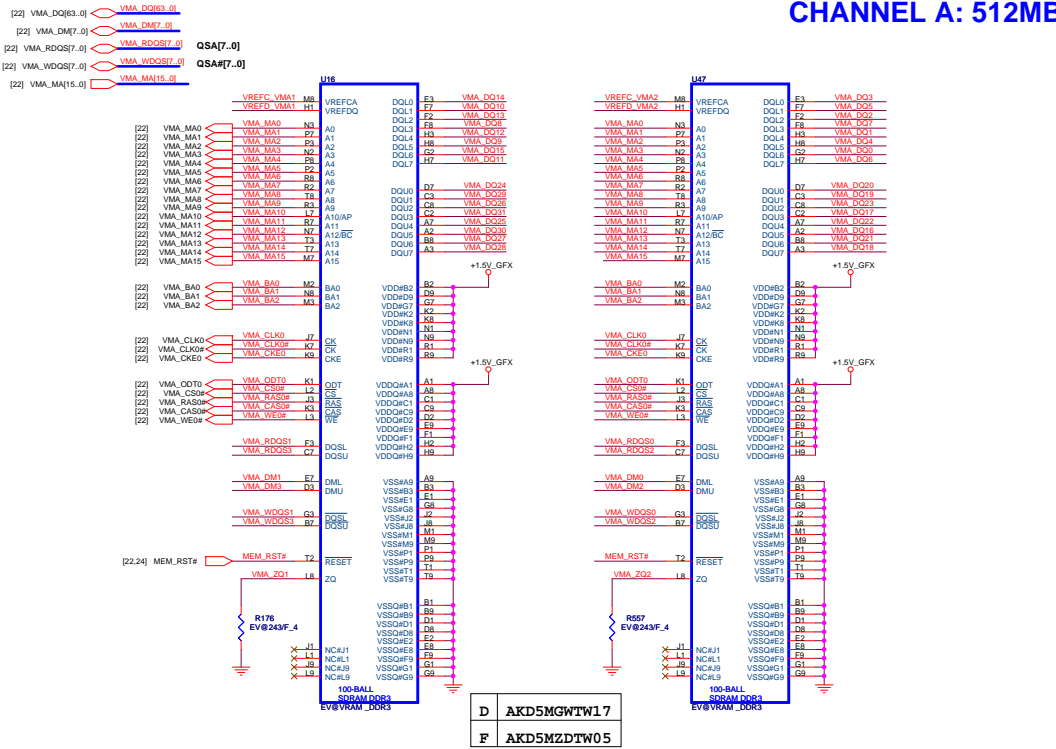
Place MVREF dividers and Caps close to ASIC

SP : Thames Pro,XT R=240ohm(CS12402FB03)
Mars R=120ohm(CS11202FB11)

Ball Name	Thames	Mars
MEM_CALRN0	240ohm	X
MEM_CALRN1	X	X
MEM_CALRN2	240ohm	X
MEM_CALRP0	240ohm	120ohm
MEM_CALRP1	X	X
MEM_CALRP2	240ohm	X



CHANNEL A: 512MB DDR3 (64M*16*4pcs)



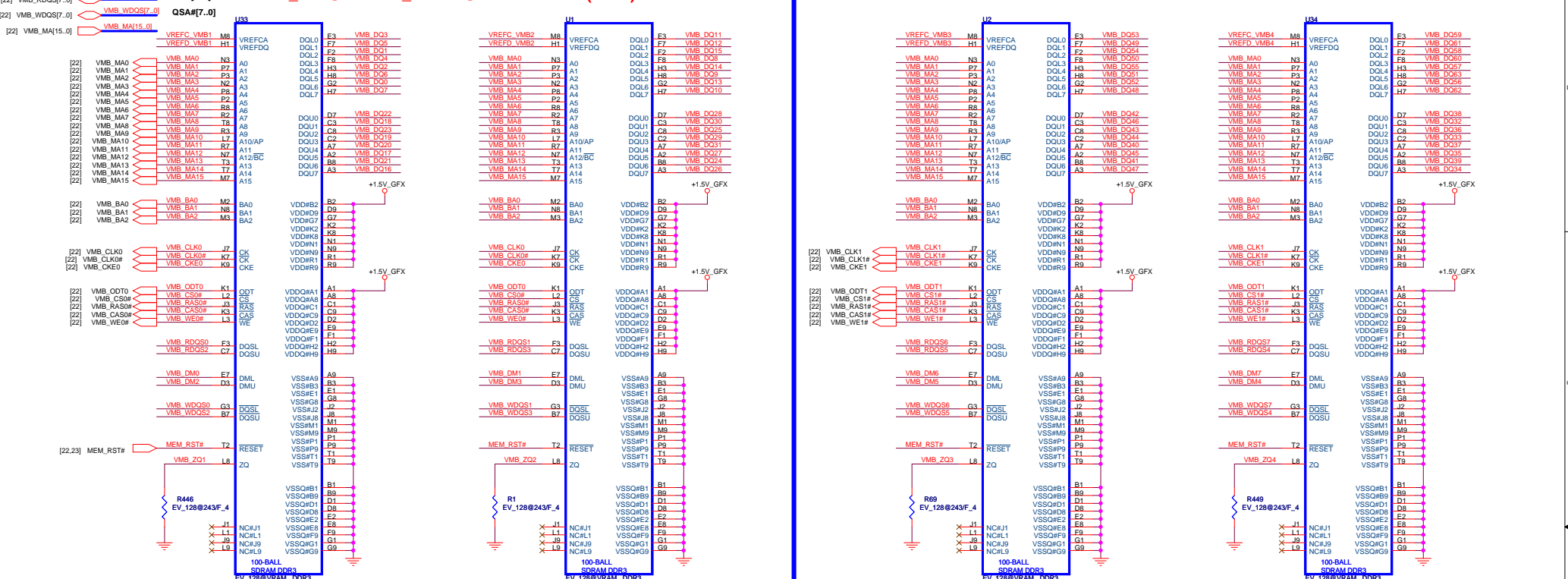
EV_Sp@ : Thames Pro,XT R=56ohm(CS05602FB15)
Mars R=40.2ohm(CS04022FB28)

EV_Sp@ : Thames Pro,XT R=56ohm(CS05602FB15)
Mars R=40.2ohm(CS04022FB28)

[22] VMB_DQ[63..0] VMB_DQ[63..0]

CHANNEL B: 512MB DDR3 (64M*16*4pcs)

[22] VMB_DM[7..0] VMB_DM[7..0] QSA[7..0] EV_128@ and EV_128SP@: Thames Pro(64bit) sku not stuff

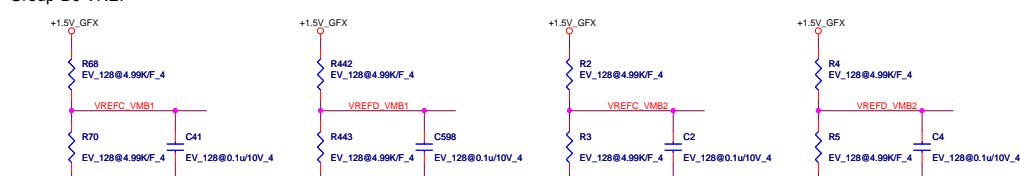


TOP Down

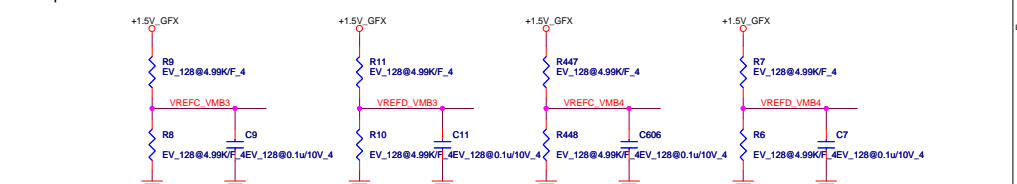
TOP Up

BOT Up

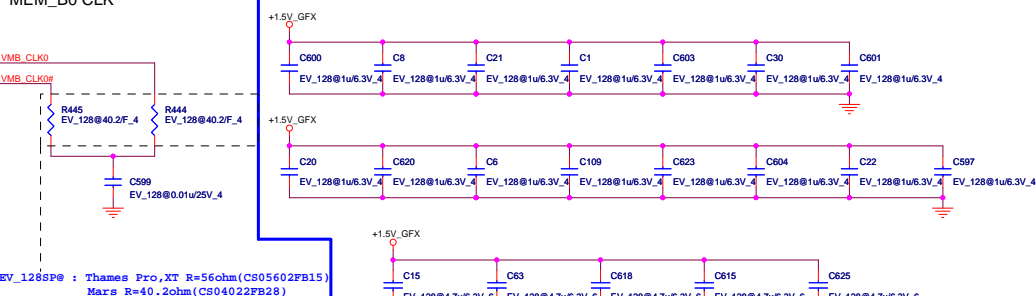
Group-B0 VREF	Group-B1 VREF
+1.5V GFX	+1.5V GFX



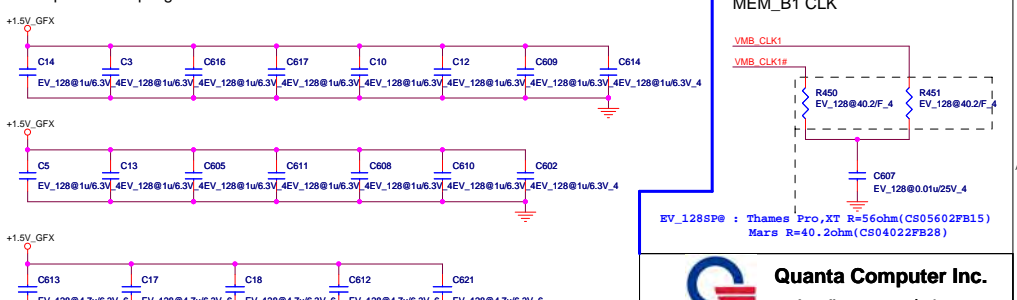
Group-B1 VREF



MEM_B0 CLK	Group-B0 decoupling CAP	Group-B1 decoupling CAP	MEM_B1 CLK
------------	-------------------------	-------------------------	------------



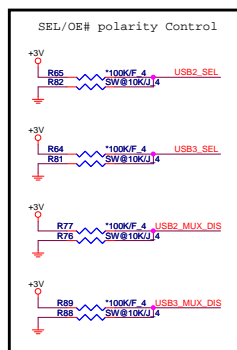
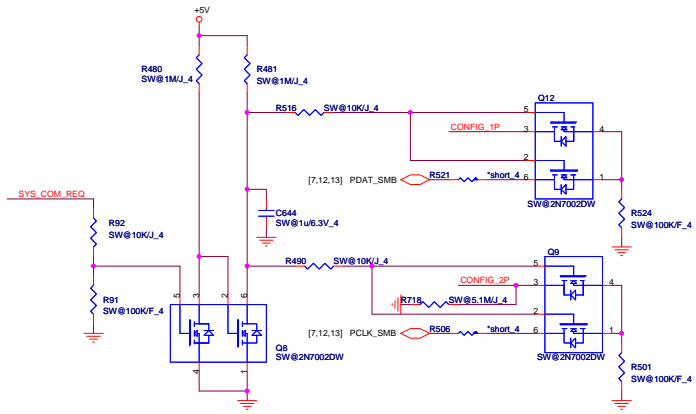
Group-B1 decoupling CAP	MEM_B1 CLK
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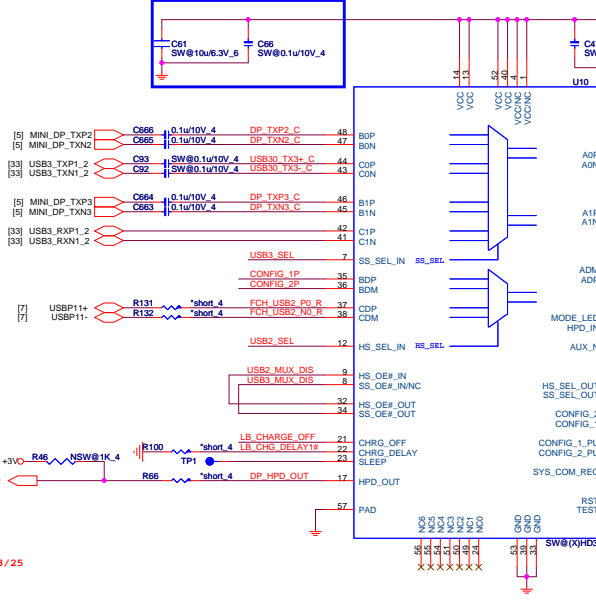
EV_128SP@ : Thames Pro,XT R=56ohm(CS05602FB15)
Mars R=40.2ohm(CS04022FB28)

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PROJECT : ZRI/ZOI

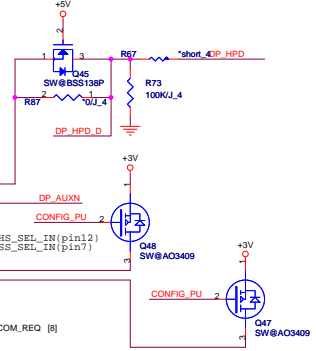
mini DP ML (DPP)



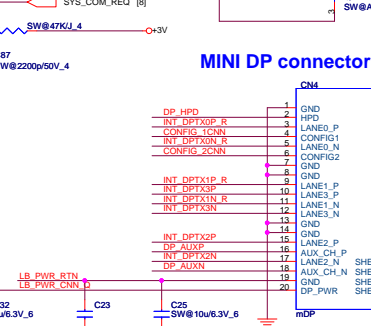
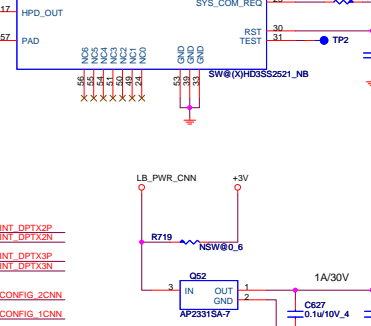
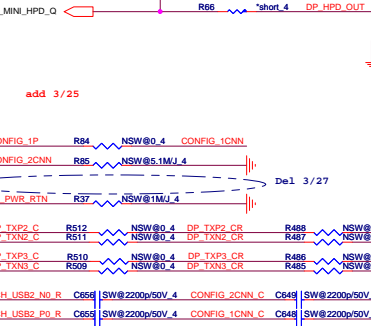
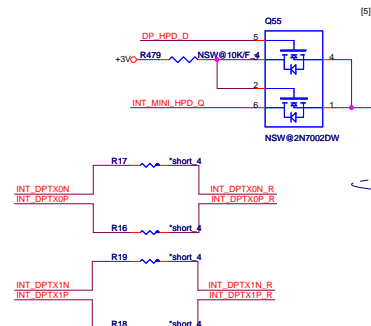
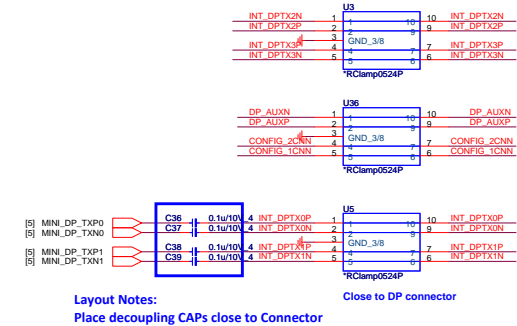
Layout Notes:
Place near Pin13 and Pin14



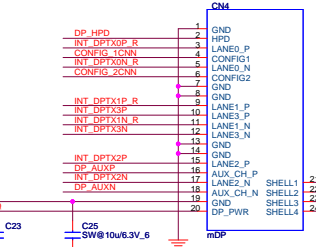
DP HPD (DPP)



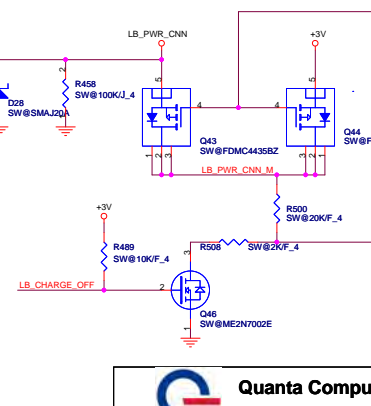
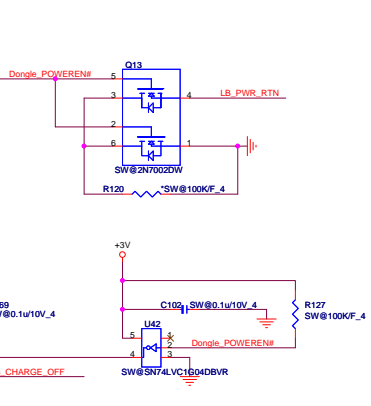
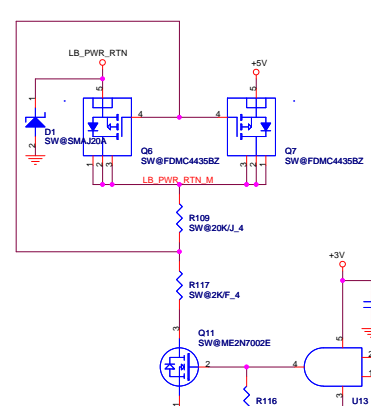
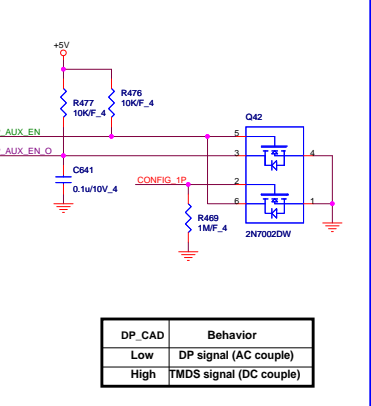
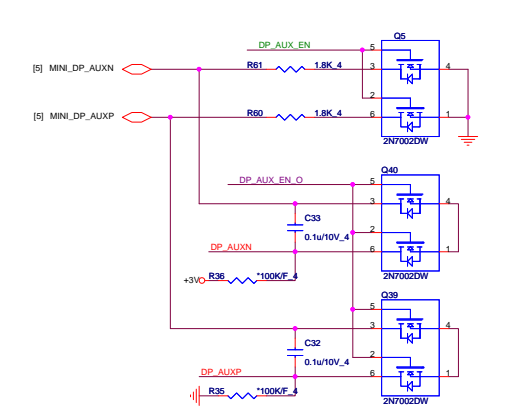
ESD Protect (EMC)



MINI DP connector (DPP)

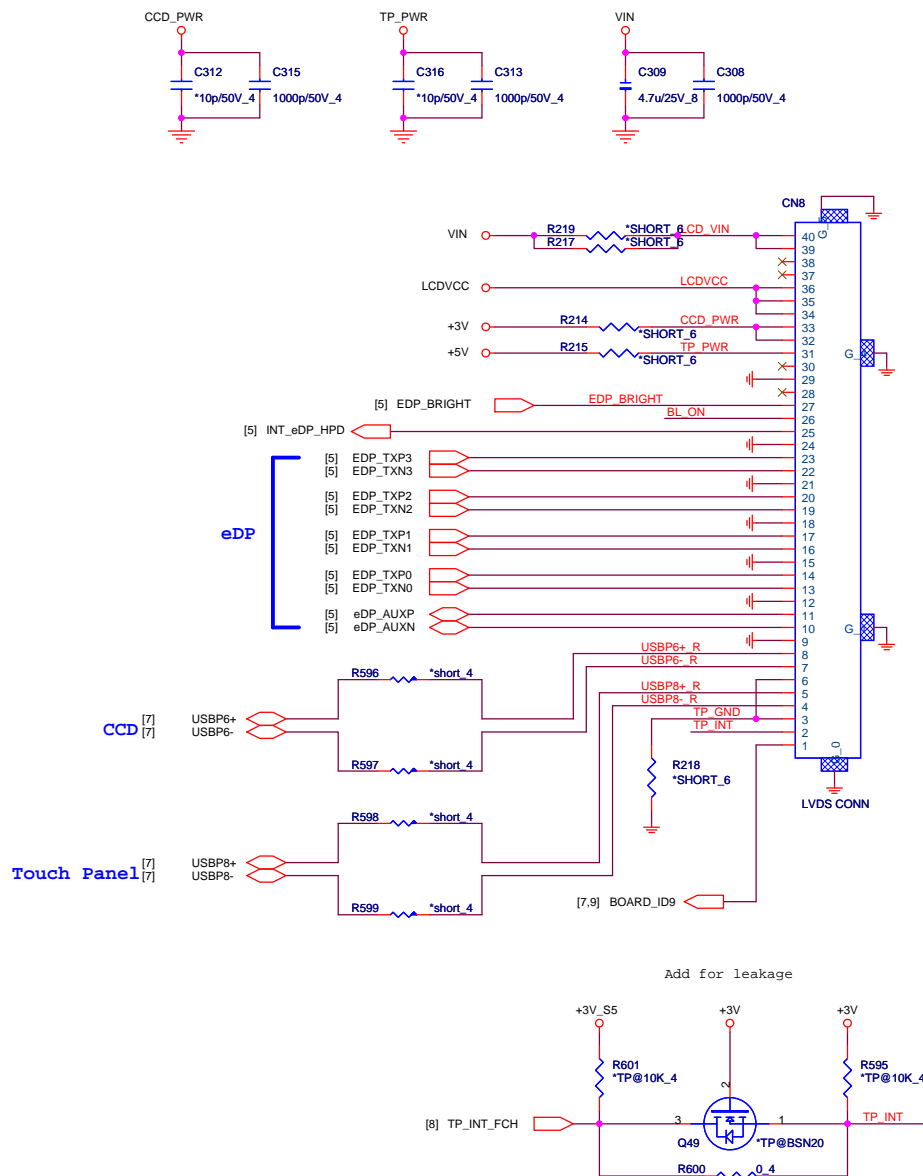


mDP AUX (DPP)

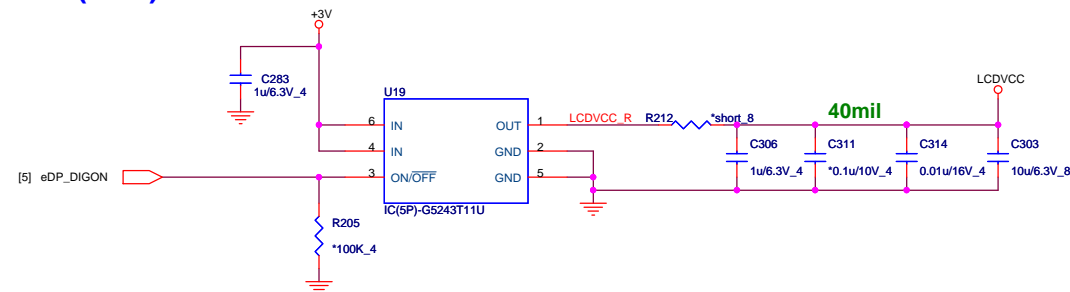


DP_CAD	Behavior
Low	DP signal (AC couple)
High	TMDS signal (DC couple)

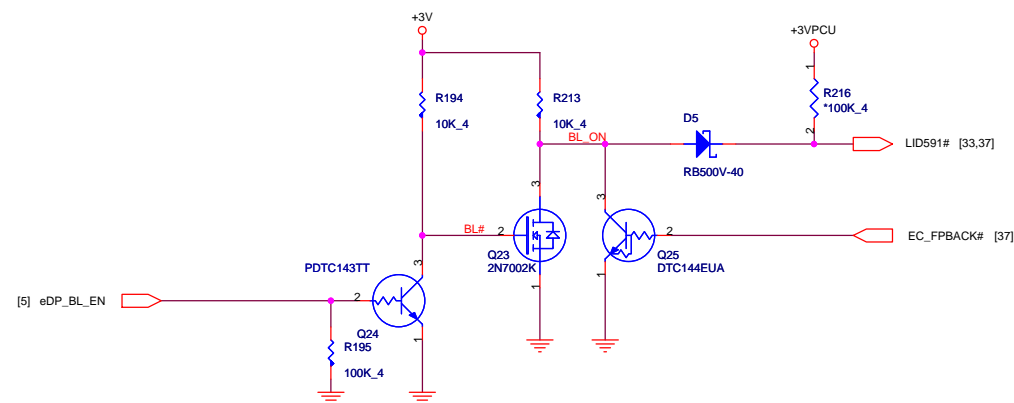
eDP(LDS)



LCD PW(LDS)

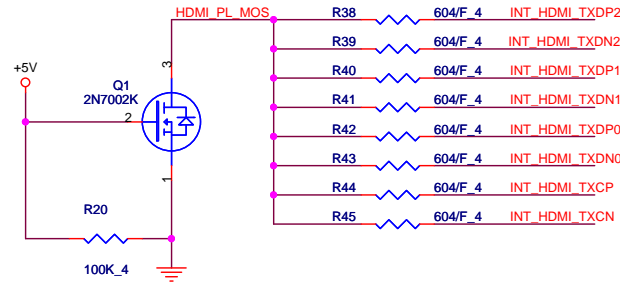
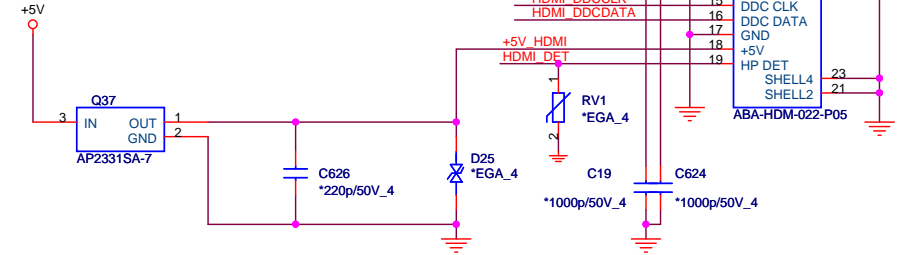
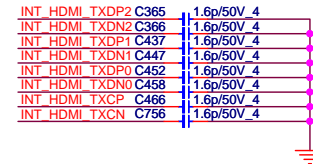
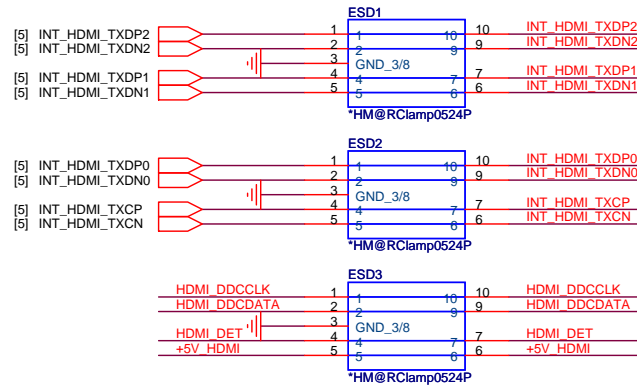


Backlight Control(LDS)



HDMI

ESD

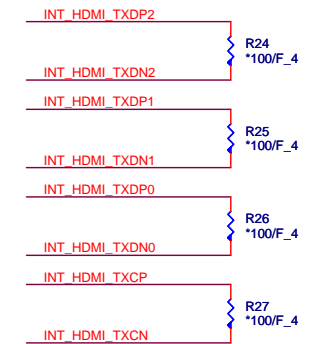


HDMI SDVO I2C Control

HDMI HPD SENSE

EMI reserve for HDMI(EMC)

Close connector



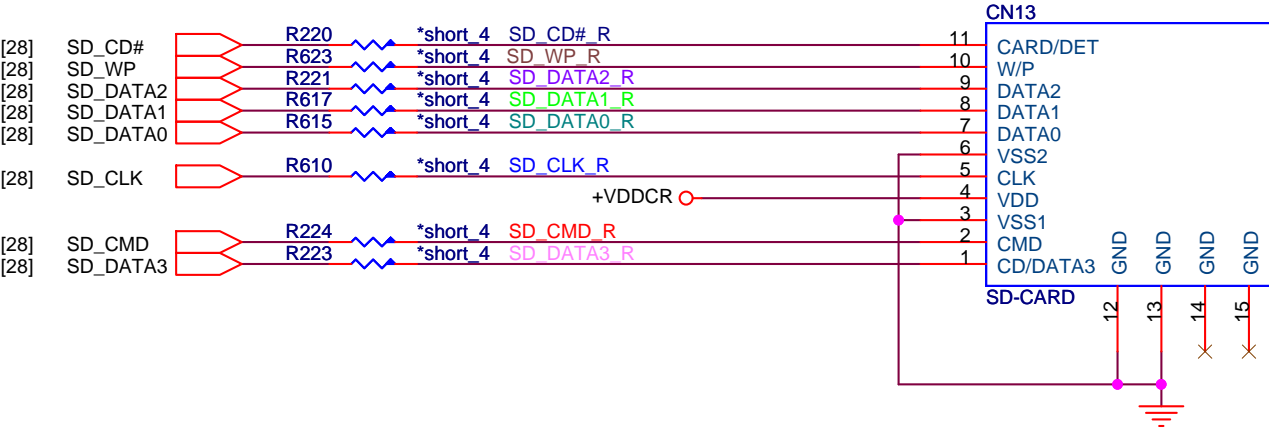
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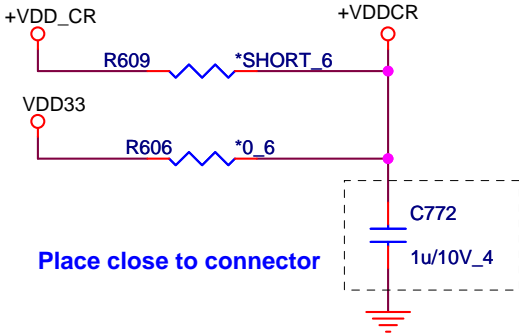
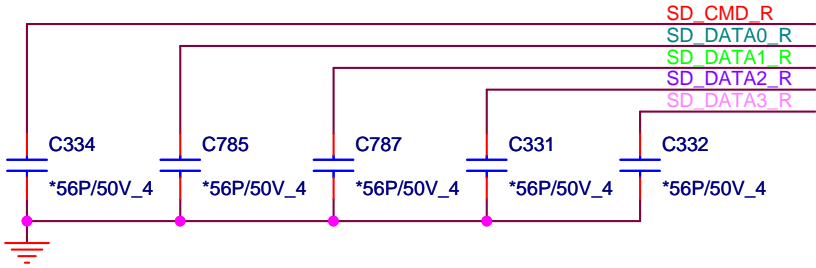
Size	Document Number	Rev
	HDMI	A1A
Date: Wednesday, April 24, 2013	Sheet 27 of 50	

CARD READER CONNECTOR (MMC)

SD/MMC CARD READER (MMC)



EMI



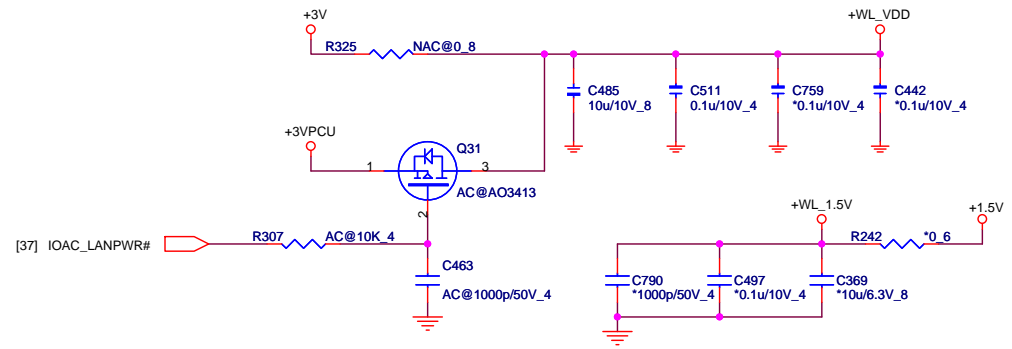
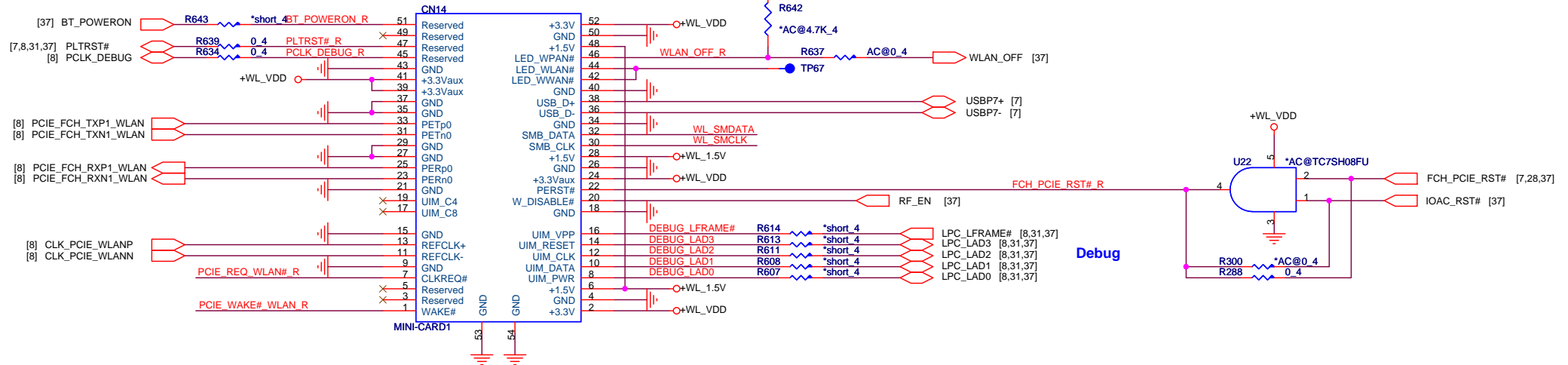
Quanta Computer Inc.

PROJECT : ZRI/ZQI

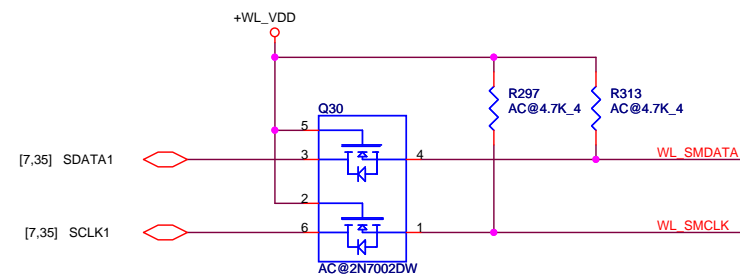
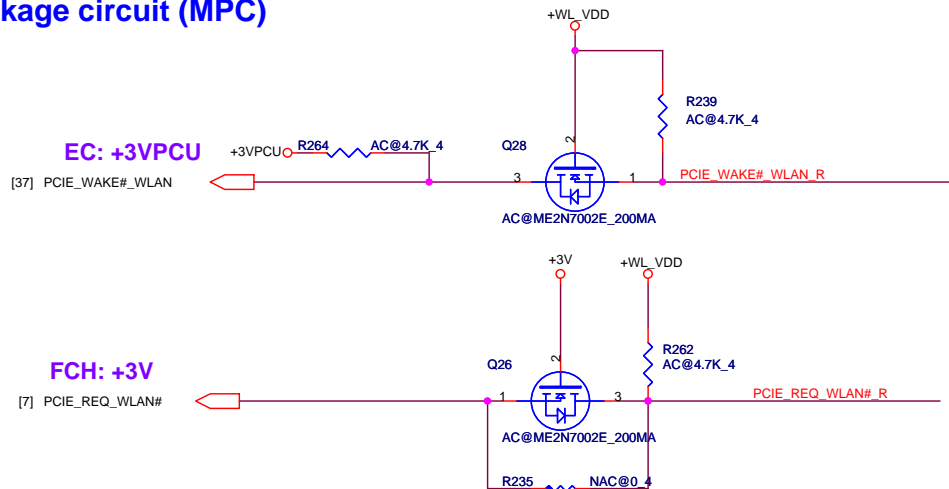
Size	Document Number	Rev
	CARD READER CONNECTOR	A1A

MINI-CARD WLAN&BT(MPC)

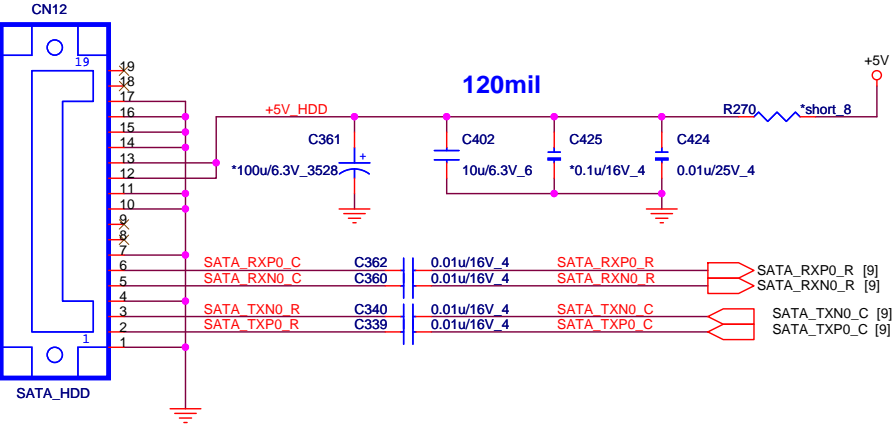
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA



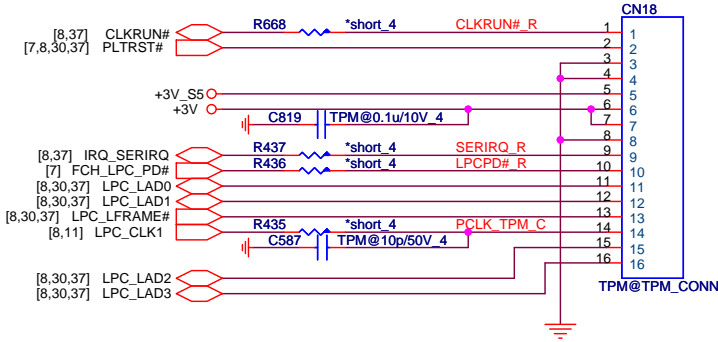
Leakage circuit (MPC)



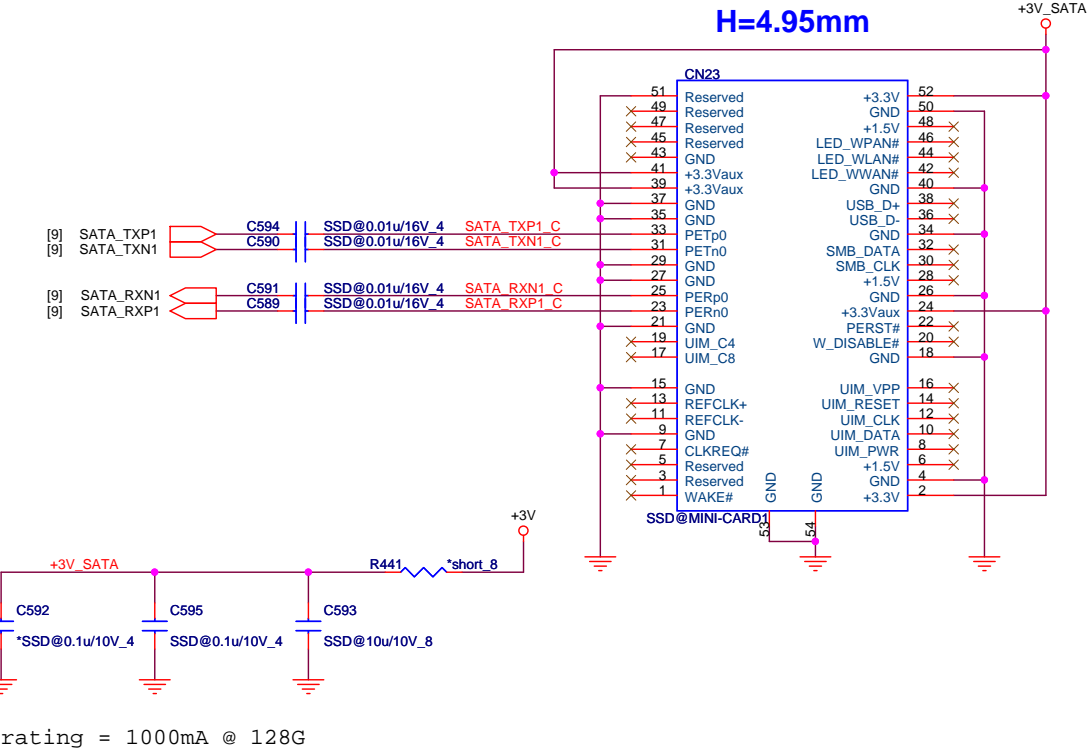
SATA HDD



TPM

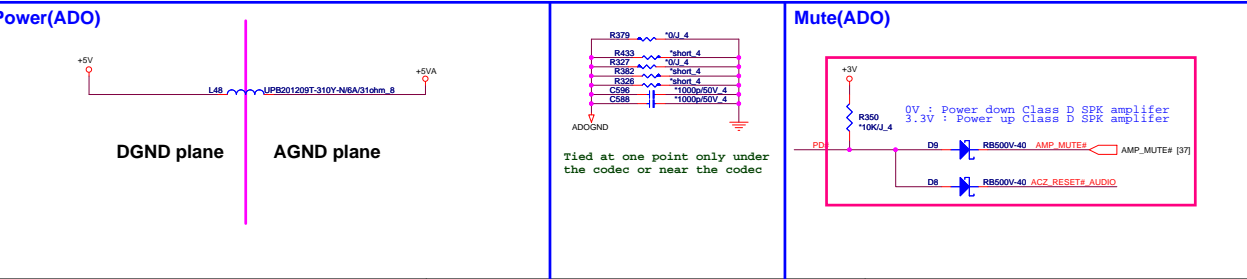
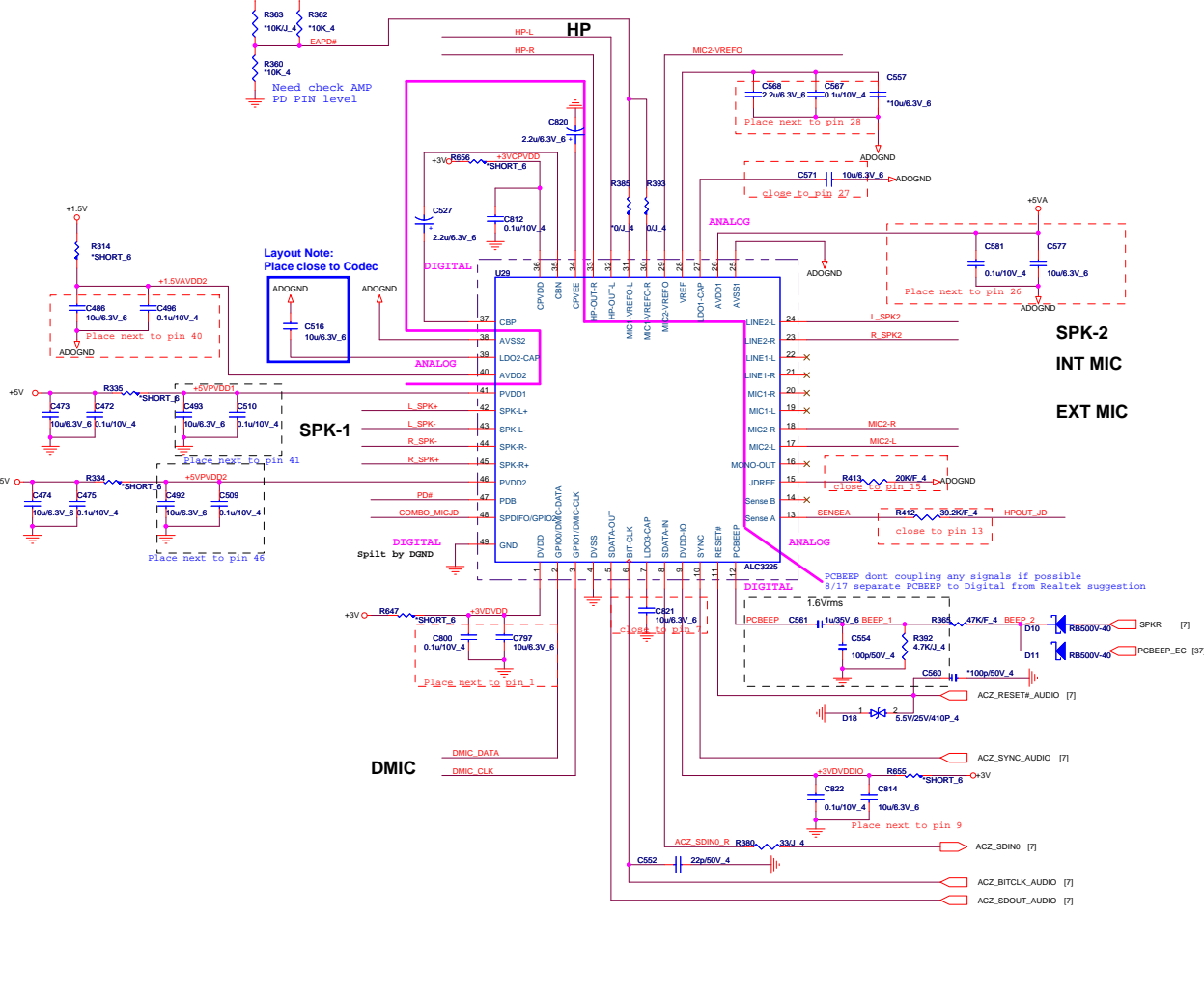


MINI-CARD SSD

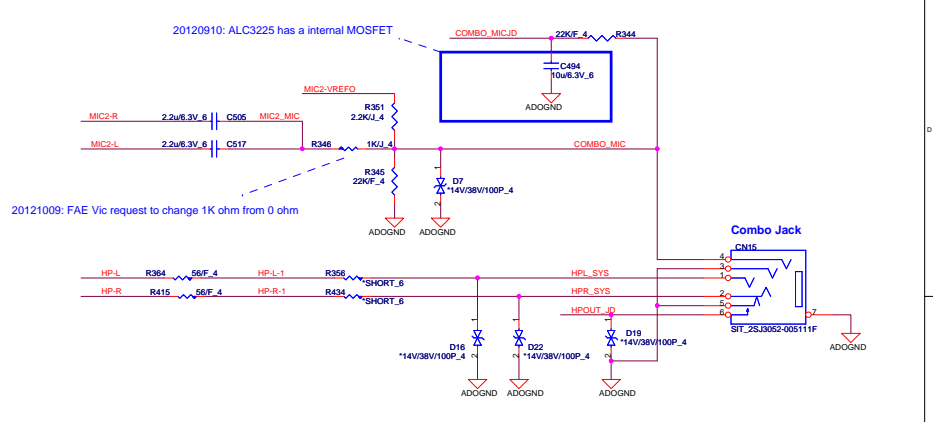


SATA Re-driver

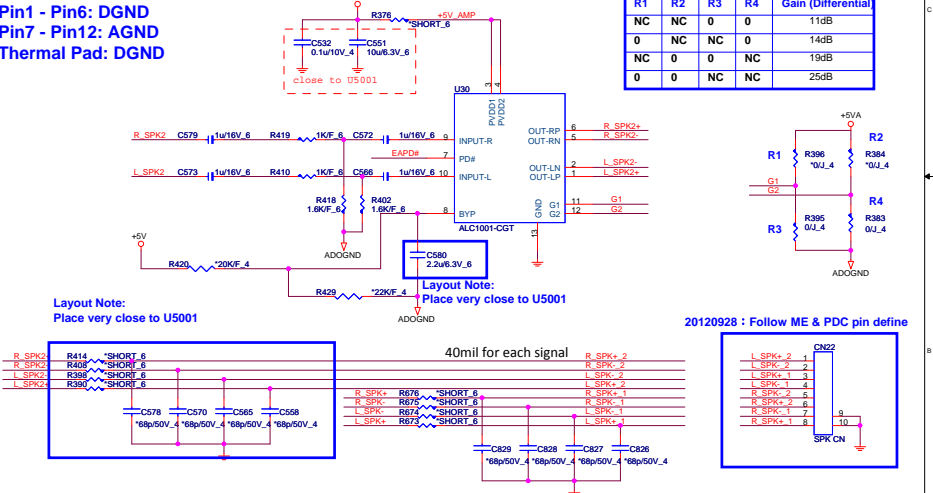
Codec (ADO)



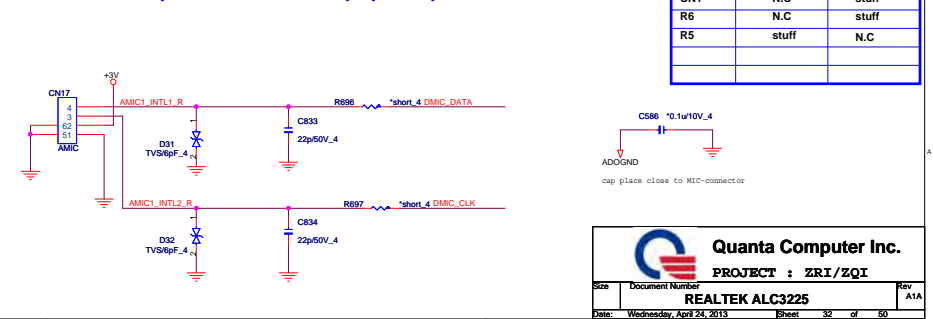
HEADPHONE/Mic combo (AMP)



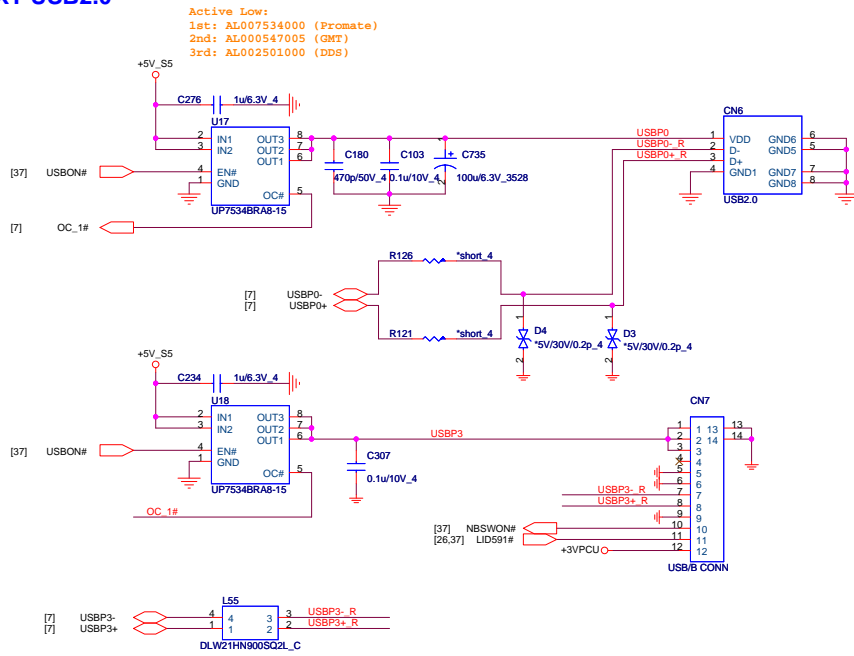
Internal Speaker (AMP)



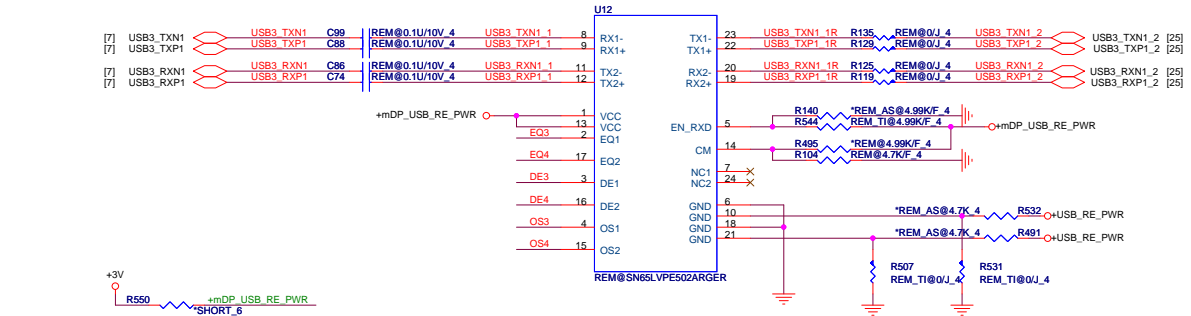
INT DIP AMIC(Reserve Stereo) (AMP)



INT & EXT USB2.0

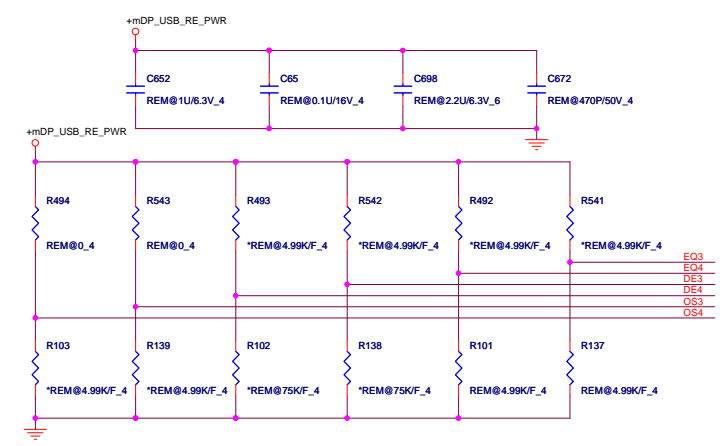


mDP USB3.0 re-driver IC



USB3_RXP1 R515 NREM@0/J_4 USB3_RXP1_2
USB3_RXN1 R516 NREM@0/J_4 USB3_RXN1_2
USB3_TXN1 R525 NREM@0/J_4 USB3_TXN1_2
USB3_TXP1 R522 NREM@0/J_4 USB3_TXP1_2

Control pins setting			
EN_RXD	Device function	CM	Device function
1(default)	Normal Operation	0(default)	Normal Operation
0	Sleep Mode	1	Compliance Test Mode

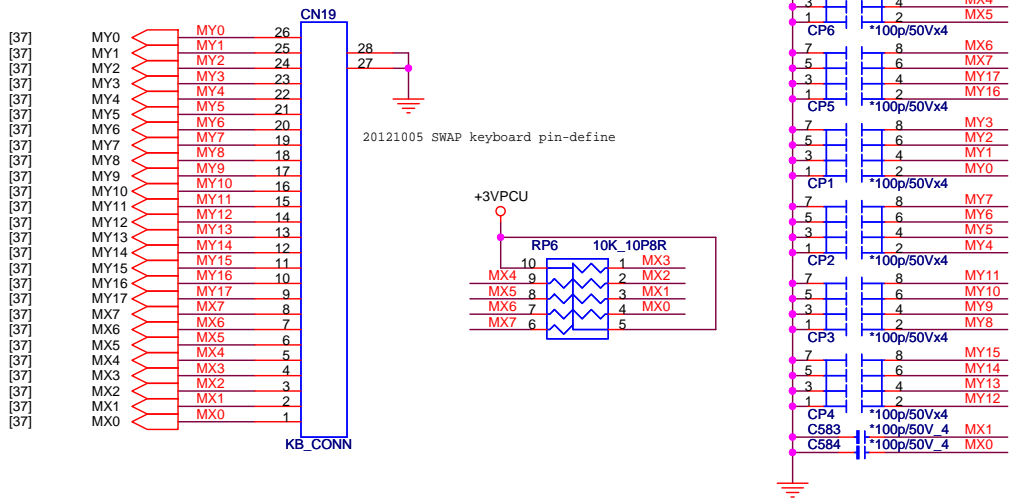


USB3.0 re-driver IC

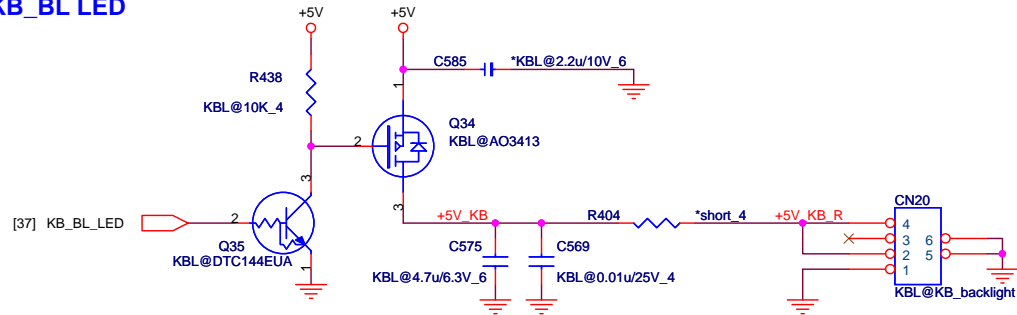


Figure 1: USB to UART bridge circuit diagram. The diagram shows a USB to UART bridge IC (U6, CH@SLG55584A) connected to a USB port and a UART port. The USB port is connected to BC_CEN, USBP10+/-C, and USBP10+/-V. The UART port is connected to USB3_TXN0 R, USB3_TXP0 R, and USB3_RXN0 R. The IC is also connected to a 5VPCU supply and a 10K resistor (R482). The circuit includes various pull-up and pull-down resistors (R93, R76, R472, R471, R466, R478, C50, C62) and capacitors (C50, C62). The IC is labeled U6, CH@SLG55584A, and the UART port is labeled U38, CH@TC7SH08FU.

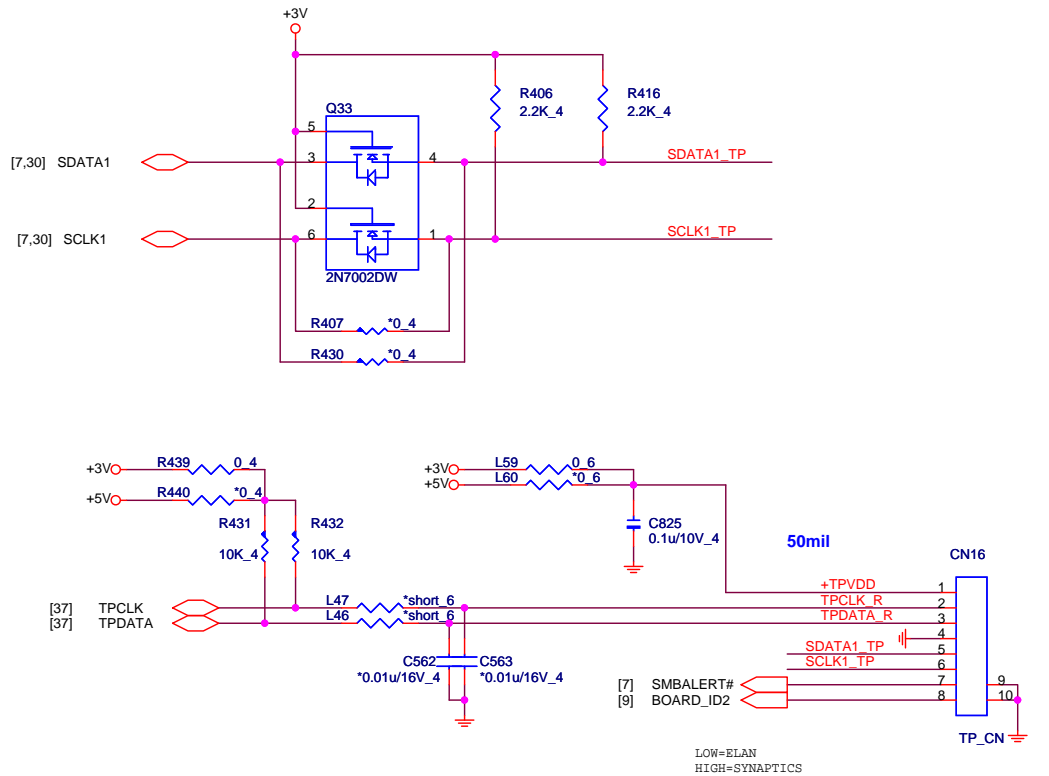
K/B(KBC)



KB_BL LED

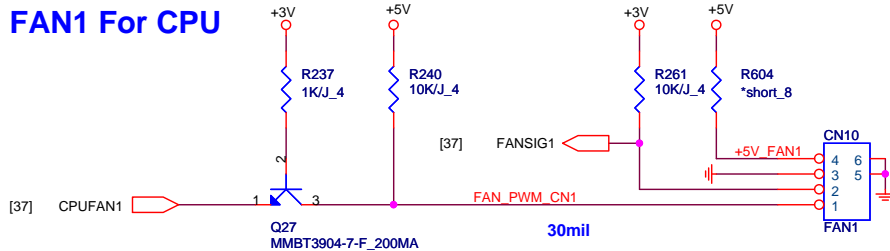


TOUCHPAD BOARD CONN(TPD)



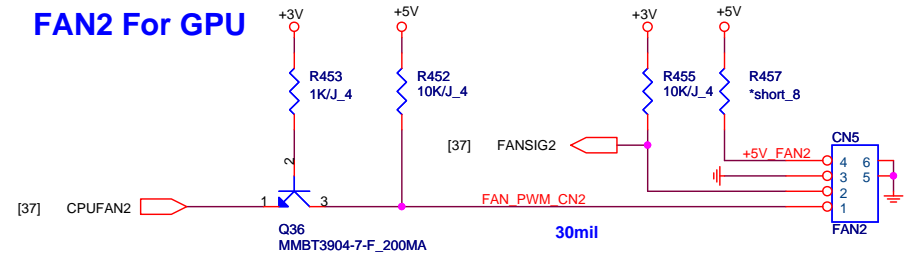
CPU FAN(THM)

FAN1 For CPU



If need to support XT(25) GPU, need check with thermal

FAN2 For GPU



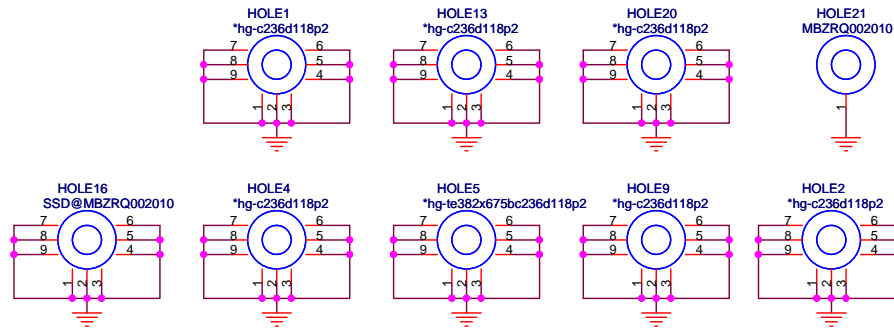
Quanta Computer Inc.

PROJECT : ZRI/ZQI

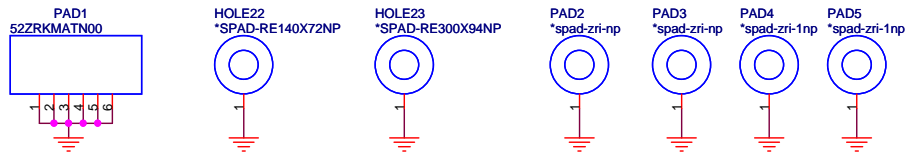
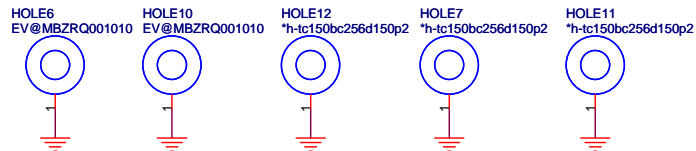
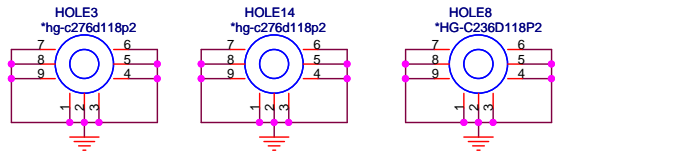
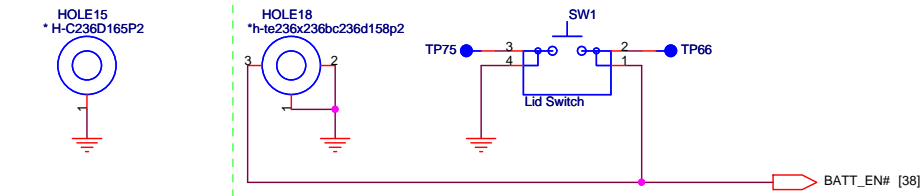
Size	Document Number	Rev
	KB/TP/FAN	A1A

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HOLE(OTH)

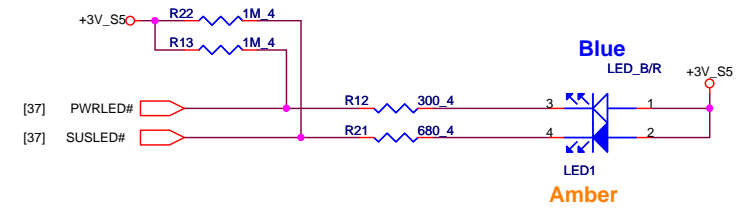


BATT Enable short pad

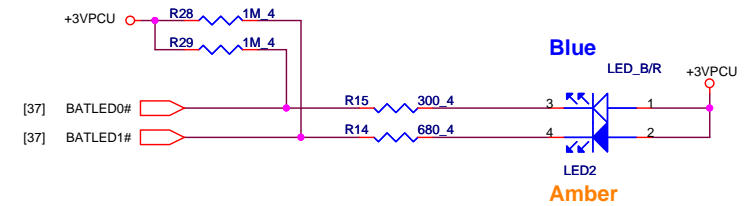


LED(UIF)

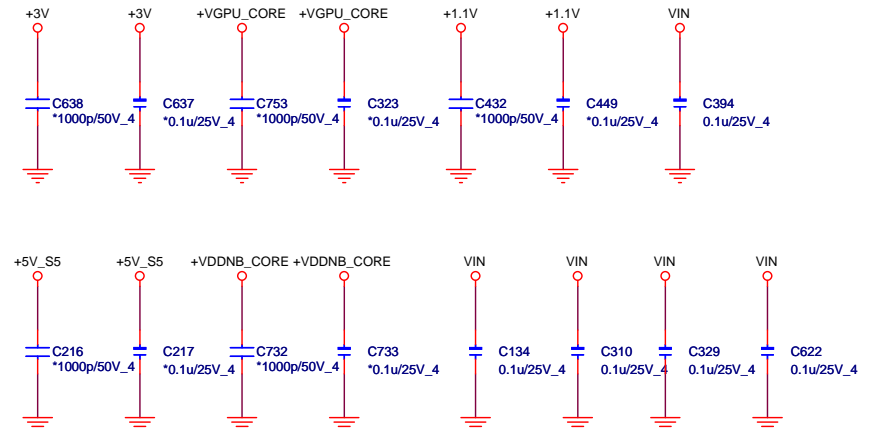
Power



Battery



EE RETURN-PATH CAPACITORS(EMC)

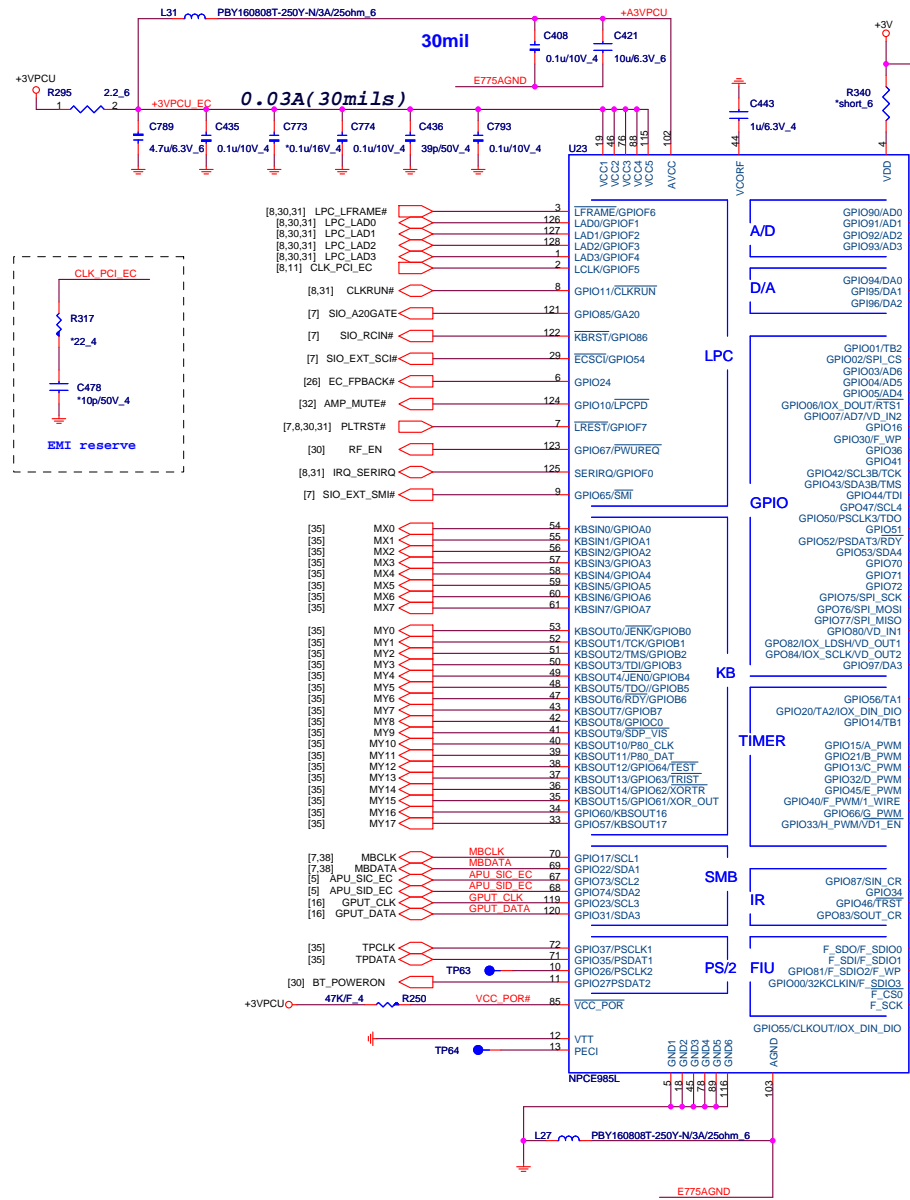


Quanta Computer Inc.

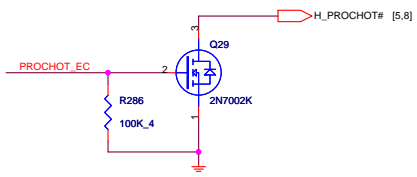
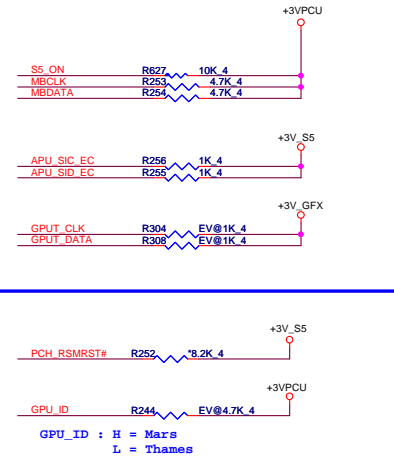
PROJECT : ZRI/ZQI

Size	Document Number	Rev
	LAN DB/ LED/ EMI/ Hole	A1A
Date:	Wednesday, April 24, 2013	Sheet 36 of 50

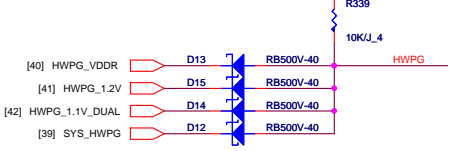
EC(KBC)



SM BUS PU(KBC)



HWPG(KBC)



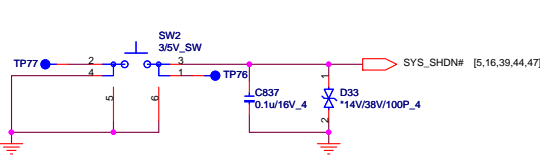
SM BUS ARRANGEMENT TABLE

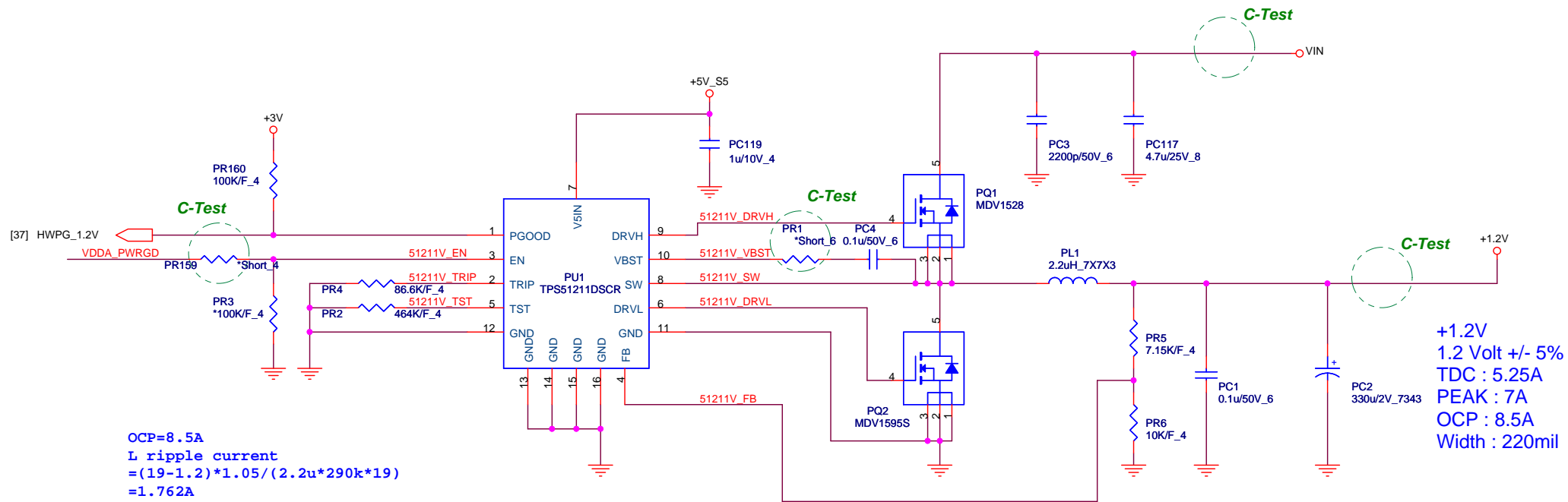
SM Bus 1	Battery, FCH
SM Bus 2	APU
SM Bus 3	GPU

Placement for EC of VIN power plan



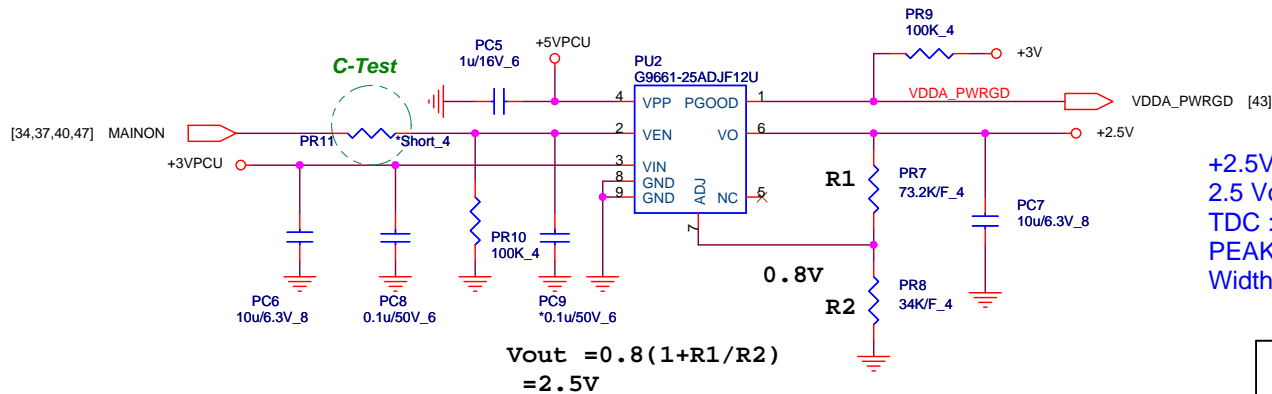
3/5VPCU reset switch (CLG)





OCP=8.5A
 L ripple current
 $= (19-1.2) \times 1.05 / (2.2 \times 290 \times 19)$
 $= 1.762A$
 $V_{trip} = 8.5 - (1.762/2) \times 14mohm$
 $= 0.10666V$
 $R_{limit} = 0.10666 / 10uA \times 8 = 85.322Kohm$

+1.2V
 1.2 Volt +/- 5%
 TDC : 5.25A
 PEAK : 7A
 OCP : 8.5A
 Width : 220mil



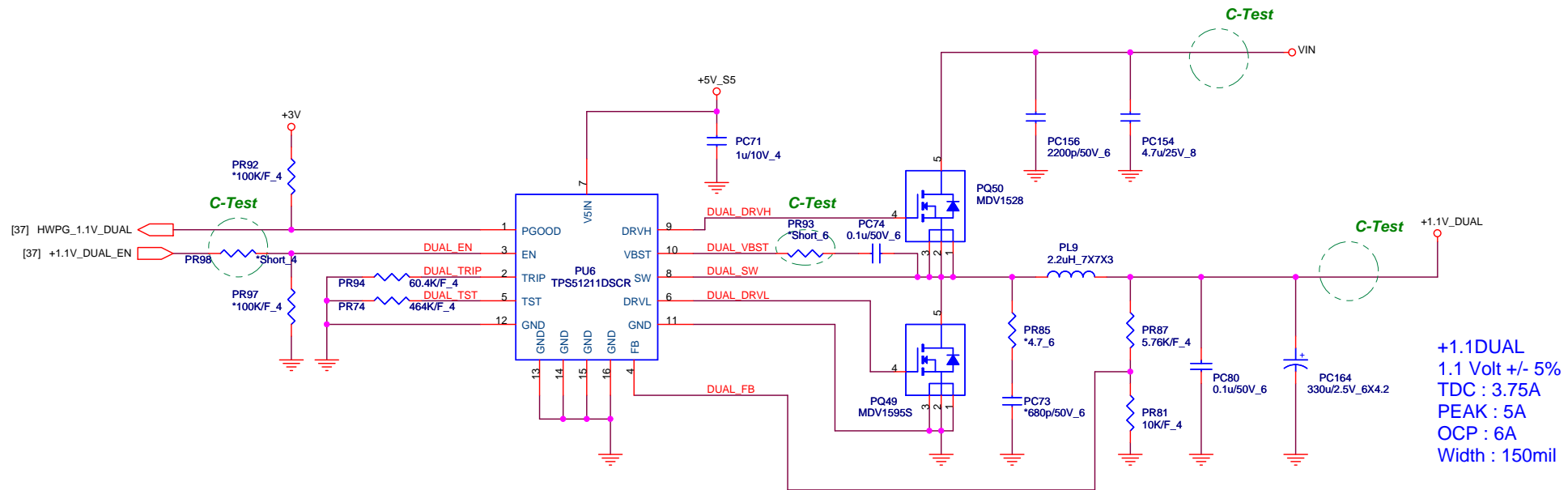
+2.5V
 2.5 Volt +/- 5%
 TDC : 0.6A
 PEAK : 0.75A
 Width : 40mil

$$V_{out} = 0.8 (1 + R1/R2) = 2.5V$$

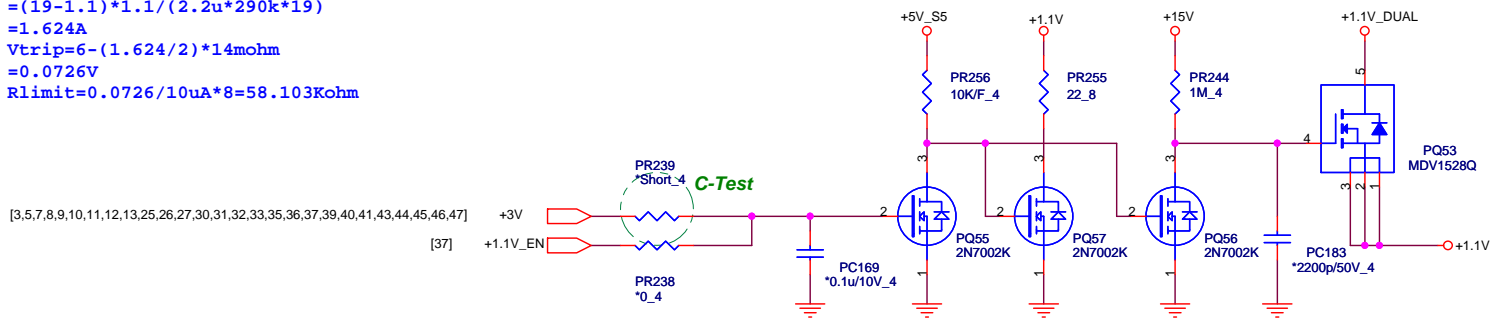
Quanta Computer Inc.

PROJECT : ZRI/ZQI

Size	Document Number	Rev
	+1.2V(TPS51211)/+2.5V	A1A
Date:	Wednesday, April 24, 2013	Sheet 41 of 50



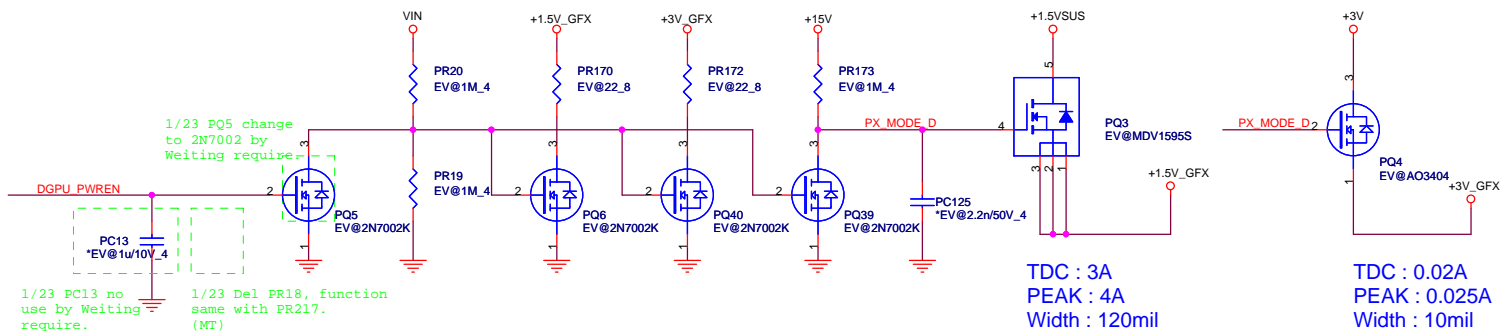
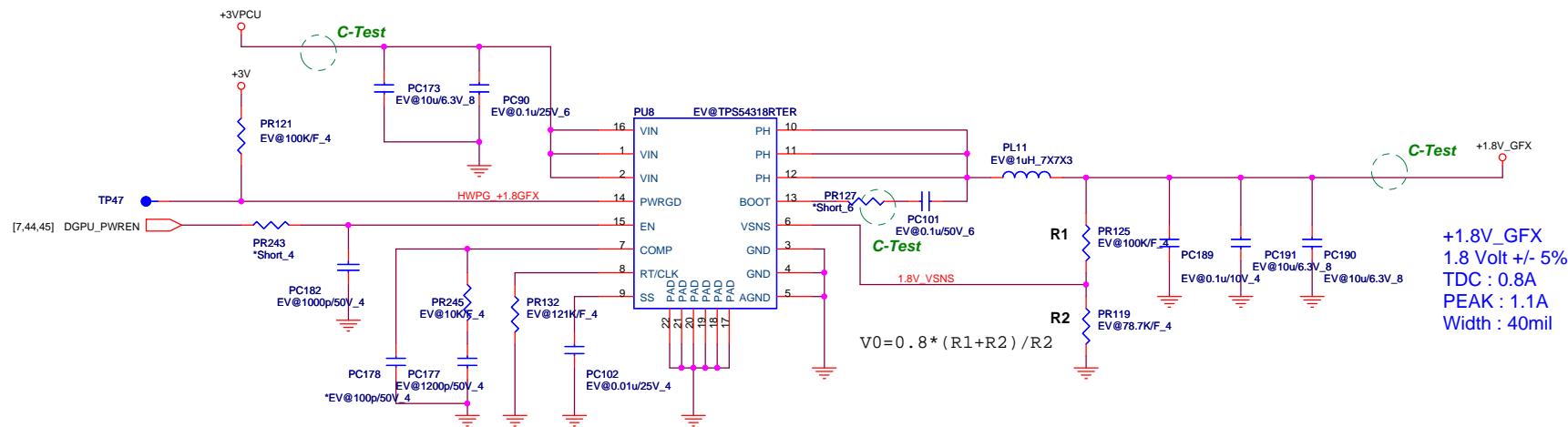
OCP=6A
 L ripple current
 $= (19-1.1) \cdot 1.1 / (2.2 \mu \cdot 290k \cdot 19)$
 $= 1.624A$
 $V_{trip} = 6 - (1.624/2) \cdot 14mohm$
 $= 0.0726V$
 $R_{limit} = 0.0726 / 10 \mu A \cdot 8 = 58.103Kohm$



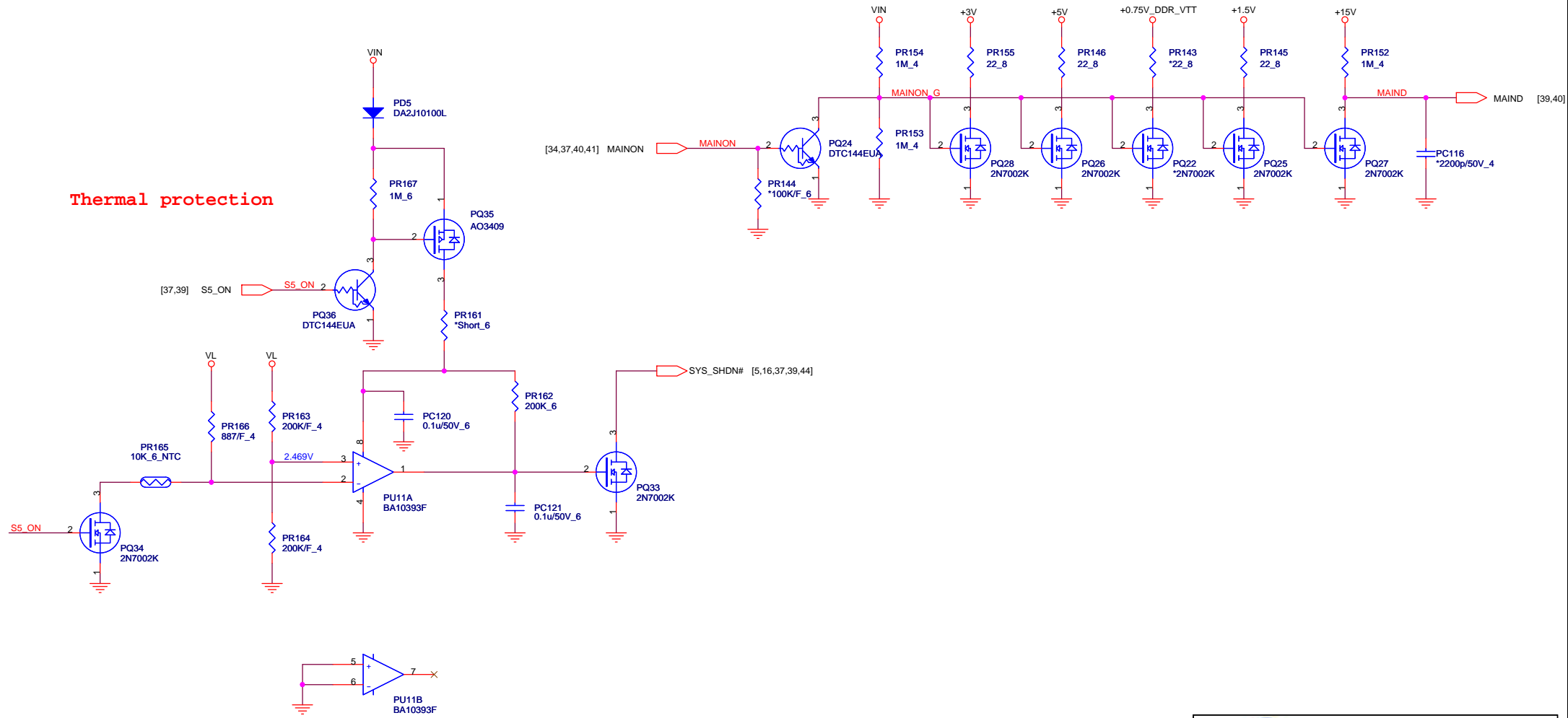
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PROJECT : ZRI/ZQI

Size	Document Number	Rev
	+1.1V_DUAL(TPS51211)	A1A
Date:	Wednesday, April 24, 2013	Sheet 42 of 50

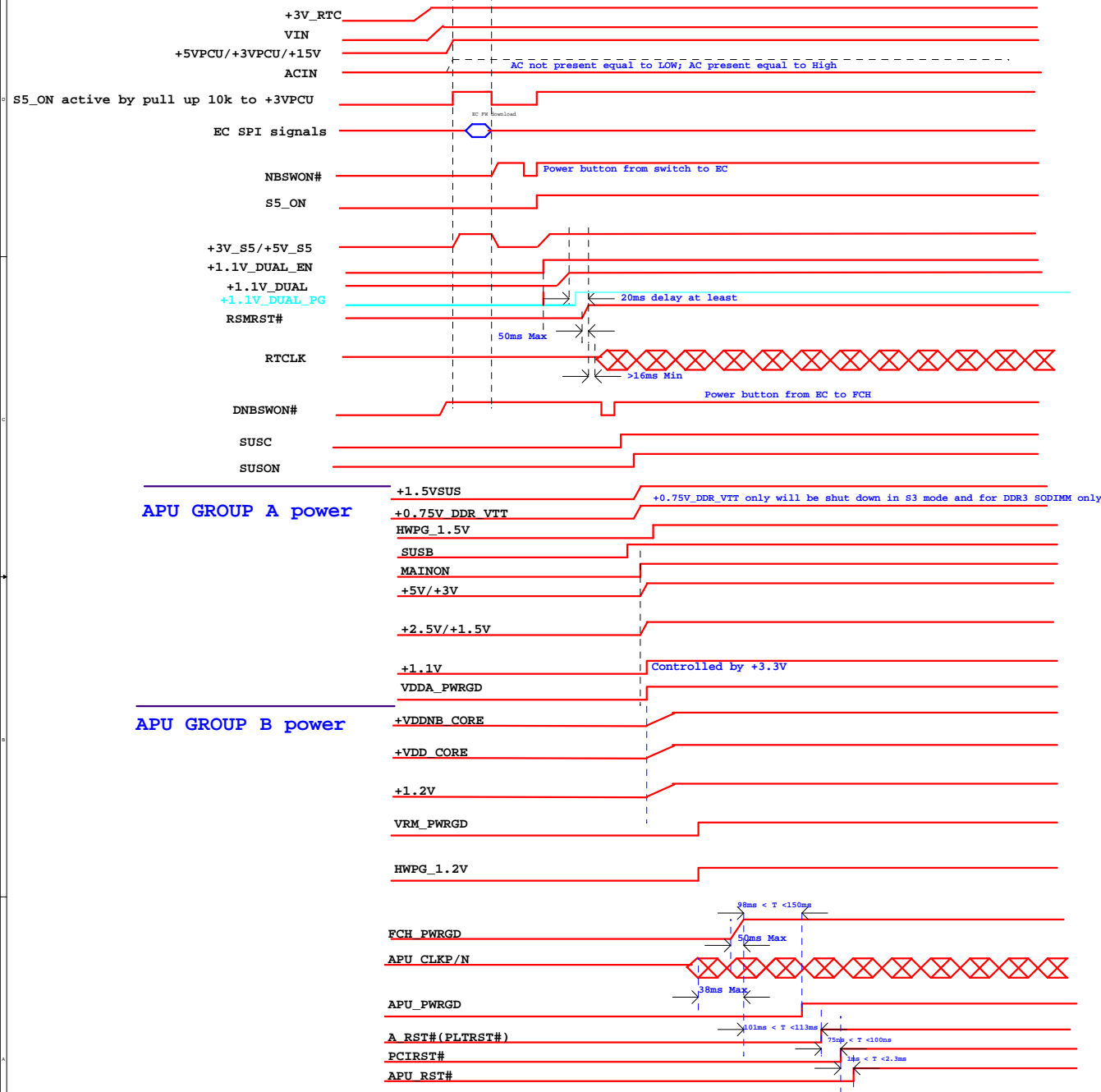


Thermal protection



For EC control thermal protection (output 3.3V)

ZRP Power On Sequence: S5 > S0



APU Power on sequence required:

Llano APU:

1.Group A (+1.5VSUS, +2.5V_VDDA) ramp before Group B
(+VDD_CORE, +VDDNB_CORE, +1.2V_VDDPR)

HUDSON-M3:

1.+3V_S5 ramp before +1.1V_DUAL
2.+3V ramp before +1.1V
3.+3V_S5,+3V ramping down time > 300us
4.100us <= +3V_S5,+3V <= 40ms
5.100us <= All power rails except +3V_S5,+3V <= 40ms

Power Tree Table

